R.T.
YILDIZ TECHNICAL UNIVERSITY
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCE

REALIZATION OF ULTRAWIDEBAND LINEAR MICROWAVE LOW NOISE AMPLIFIER

ARSLAN CHARIYEV

MASTER'S DEGREE THESIS
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
COMMUNICATIONS DIVISION

ADVISOR
PROF. DR. FİLİZ GÜNEŞ

ISTANBUL, 2011

R.T.

YILDIZ TECHNICAL UNIVERSITY
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCE

REALIZATION of ULTRAWIDEBAND LINEAR MICROWAVE LOW NOISE AMPLIFIER

It is hereby approved and proclaimed on 12.01.2012 by the members of the commission, whose names are indicated below, that the thesis prepared by Arslan CHARIYEV is acknowledged and admitted as **MASTER'S DEGREE THESIS** at Electronics and Communications Engineering Department of Graduate School of Natural and Applied Science of the Yıldız Technical University.

Thesis Advisor

Prof. Dr. Filiz GÜNEŞ

Yıldız Technical University

Members of Commis-sion

Prof. Dr. Filiz GÜNEŞ

Yıldız Technical University _____

Asst. Prof. Dr. Hamit TORPİ

Yıldız Technical University _____

Asst. Prof. Dr. Erdal KORKMAZ

Fatih University _____

ACKNOWLEDGEMENT

The preparation of this paper has depended on my lengthy research and a number of very supportive individuals, without whom this paper would not have come into being. First of all, I would like to thank my university advisor Prof. Dr. Filiz GÜNEŞ, and Asst. Prof. Dr. Salih DEMİREL for their invaluable and immeasurable academic support and encouragement. They always guided me through hardships and difficulties I faced. I would like to also thank the UEKAE team, especially Feyzullah YAYIL, whose support enabled me to overcome barriers and constrains.

Most importantly, I want to express my deep appreciation to my mother, Toraýeva Zulfiýa KOÇİÝEVNA, and fiancée, Suna KARAKURT, for their encouragement, endurance, devotion and support. Their unfaltering patience and understanding allowed me to work during many evenings, holidays, and weekends to complete this task. And finally, I want to express my gratitude to everyone how had believed in me and ordained their endless support.

December, 2011

Arslan CHARIYEV

CONTENTS

Pages

LIST OF SYMBOLS

C/ C_{un}	Capacitor/Unit Capacitor
G/ G_{un}	Conductor/Unit Conductor
GHz	Giga Hertz
G_T	Transduce Gain
I_D	Drain Current
L/ L_{un}	Inductor/Unit Inductor
NF	Noise Figure
R/ R_{un}	Resistor/Unit Resistor
R_n	Equivalent Noise Resistor
V_{DS}	Drain to Source Voltage
ε_{eff}	Effective dielectric constant
Ω	Ohm

LIST OF ABBREVATIONS

ANG	Angle
BJT	Bipolar Junction Transistors
BW	Bandwidth
CAD	Computer Aided Design
DC	Direct Current
FET	Field Effect Transistor
HBT	Hetero-junction Bipolar Transistors
HEMT	High-Electron-Mobility Transistors
LNA	Low Noise Amplifier
MAG	Magnitude
MESFET	Metal-Semiconductor Field Effect Transistor
MICs	Microwave Integrated Circuits
SRF	Self-Resonant Frequency
Sub.	Substrates
TEM	Transverse Electromagnetic Mode
VSWR	Voltage Standing Wave Ratio

LIST OF FIGURES

Pages

LIST OF TABLES

Pages

ABSTRACT

REALIZATION of ULTRAWIDEBAND LINEAR MICROWAVE LOW NOISE AMPLIFIER

Arslan CHARIYEV

Department of Electronics and Communications Engineering

McS. Thesis

Advisor: Prof. Dr. Filiz GÜNEŞ

During the last decade, stimulated by unprecedented growth in the wireless communication application, outstanding progress has been made in the development of low-cost solutions for front-end RF and microwave systems. This growing demand has further forced microwave amplifiers to widen their bandwidth. Widening bandwidth has become a pressing issue for microwave circuit designers. Today, broadband and ultra-wideband amplifiers are one of most researched topics of microwave engineering.

In this study, I aimed to design an ultra-wideband low noise amplifier utilizing in-hand technology. I had to take in to consideration to what I could reach, and that, inevitably, had a huge impact on my design and realization process. In the paper I firstly focused on theoretical background of microwave amplifier design. Then, I had demonstrated that PSO can be successfully employed for a design of matching circuit for ultra-wideband applications. In this work I had extensively utilized PSO code developed by Asst. Prof. Dr. Salih DEMİREL and Prof. Dr. Filiz GÜNEŞ.

Key words: Noise, transducer gain, VSWR, microstrip lines, S parameters, matching circuit, particle swarm optimization, stability, performance triples

ÖZET

GENİŞBAND LİNER DÜŞÜK GÜRÜLTÜLÜ KUVVETLENDİRİCİ MİKRODALGA DEVRESİNİN GERÇEKLEMESİ

Arslan CHARIYEV

Elektronik ve Haberleşme Mühendisliği Anabilim Dalı

Yüksek Lisans Tezi

Tez Danışmanı: Prof. Dr. Filiz GÜNEŞ

Son on yılda kablosuz haberleşme uygulamalarında şimdiye kadar hiç görülmemiş sıçramalar gerçekleştirilmiştir. Dahası, düşük maliyetli devre tasarımında akıl almaz ilerlemeler kaydedilmiş ve bu gelişmeler çerçevesinde artan talep, genişbantlı mikrodalga devrelerine olan ihtiyacı ve gereksinimi daha da şiddetli bir şekilde tetiklemekte ve artırmaktadır. Bundan dolayı ki, günümüzde genişbatlı LNA devre tasarımı en önemli aktüel konular arasına girmiştir

Bu çalışmamda ben genişbantlı düşük gürültülü liner mikrodalga devresini gerçeklemeyi amaçladım. Yazımda öncelikle mikrodalga kuvvetlendirici tasarımının teorik ve pratik alt yapısını kısaca anlattım. Daha sonra ise ben devrenin gerçekleme sürecini inceledim. Devre tasarımında sürü optimizasyon tekniğinin genişbant uygulamalarında başarılı bir şekilde uygulanabileceğini gösterdim. Çalışmamda Yrd. Doç. Dr. Salih DEMİREL ve Prof. Dr. Filiz GÜNEŞ'in geliştirdikleri PSO kodlarından yaralandım.

Anahtar Kelimeler: Gürültü, kazanç, VSWR, mikroşerit hatlar, S parametreleri, uydurma devreleri, parçacık sürü optimizasyonu, kararlılık, performans üçlüsü

CHAPTER 1

INTRODUCTION

We are living in an age of rapid growth and technological advancement. Today we have variety of applications which operate at microwave frequencies, and they are getting more diverse and ubiquitous. The most famous and renowned microwave industrial product is most probably “a microwave oven”. But in reality radars, satellites, military frequency mixers, mobile phones, and etc. are all typical examples of microwave circuit applications, and some are so critical that in war they may determine victory or defeat of an entire country.

A microwave application circuit may consist of several layers; where each layer (stage) has its own functions and duties to accomplish. A Low Noise Amplifier (LNA) layer has direct impact on gain and noise performance of the circuit. A natural consequence of this is that in almost all cases the general expectation from a LNA circuit is high gain and low noise. Furthermore, bandwidth and VSWR are also important performance merits of a microwave amplifier. Microwave amplifier design, transistor characterization, oscillation, and etc. are very complex, challenging, and yet interesting and promising topics of microwave engineering. Because of this, LNAs present a wide research topic with sea of literature available.

1.1 Literature Review

Microwave amplifier design is one most researched topics of the microwave engineering. In my research I used books and articles of prominent writers who are renowned for their pioneering research in microwave engineering field, like Filiz GÜNEŞ, Inder BAHL, George VENDELIN, Guillermo GONZALEZ, Prakash BAHARTIA, K. Gupta, Salih DEMİREL, and

etc. GÜNEŞ on her numerous articles, like [5], [6], [7], [12], [13] and etc., have shown how to overcome constrains of performance triples (G_T, V_i, and NF), opening new frontiers in microwave amplifier design. DEMİREL had brilliantly shown on [2], [9], [5] how Particle Swarm Optimization can be used to solve complex requirements of ultra and broadband circuits. GÜNEŞ's and DEMIREL's works had guided me for the most part of my research. For practical considerations I extensively employed "Microwave Solid State Circuit Design" by BAHL and BAHARTIA, "Essentials of RF and Microwave Grounding" by Eric HOLZMAN, "Microwave Transistor Amplifiers: Analysis and Design" by Gonzalez.

1.2 The Aim of the Thesis

In this research I had targeted to realize single-staged unconditionally stable ultra-wideband, namely, from 4GHz to 12GHz, linear low noise microwave amplifier. Following were taken as basis of design: targeted, or in other words required, noise figure (NFreq) is minimum noise figure (NFmin) of the active device, namely HJ-FET NE3503M04; required transducer gain (G_{Treq}) is 10 dB with ±3 dB variation. The realization of the circuit was constrained by available (in hand) technology, which had an immense impact on realization and design considerations.

1.3 Findings

It is well known that gain, nose figure, bandwidth, and standing wave ratios are inversely relational. Thus finding the best solution is quite difficult. In the paper it was shown that matching circuits can be designed by using particle swarm optimization approach; the technic which opens up new frontiers at CAD solutions.

In the paper I focused on the rudimentary building blocks and concepts of a microwave amplifier, and briefly discussed characteristics and solution technics employed during CAD. To the end of the paper the simulation results are presented, and consequently, compared with experiment's figures.

CHAPTER 2

MICROWAVE INTEGRATED CIRCUTS (MICs): *Fundamental Building Blocks*

GENERAL OVERVIEW

Microwave integrated circuits (MICs) were introduced at the mid of XX century. Since then microwave circuits have evolved significantly, and so did analysis methods which were employed to characterize them. Today there are two types of MICs in use: hybrid and monolithic circuits.

Hybrid MICs consist of both planar transmission lines and solid-state devices, like transistors and other passive components, like capacitors. In Figure 2.1 an S-band (2-4 GHz) hybrid MIC is illustrated. In practice hybrid MICs are shortly referred as MICs. Advantages of hybrid MICs are small size, light weight, easy fabrication, low cost, and high-volume production.

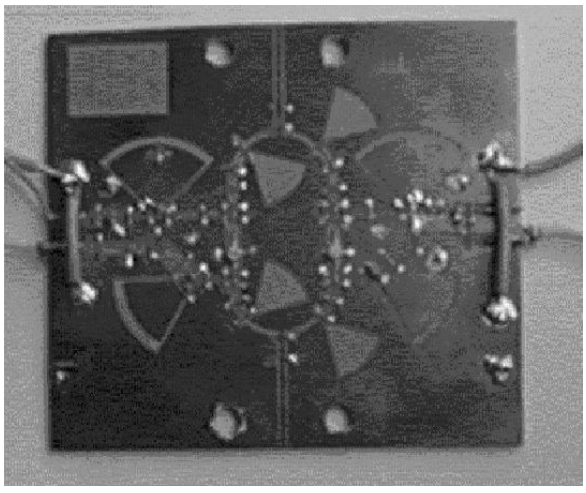


Figure 2. 1S-band (2-4 GHz) hybrid MIC push-pull FET amplifier [1].

Monolithic MICs are circuits which entirely consist of elements deposited on the semiconducting substrate; passive and solid-state elements are inclusive too. There is variety of technics employed to deposit and/or etch solid-state devices on a substrate. In the future, most microwave circuits are expected to utilize all MMICs, in particular Ka-band and millimeter-wave applications [1].

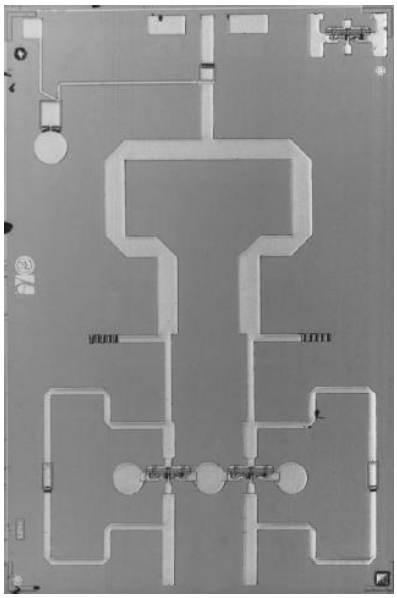


Figure 2. 2 Ka-band MMIC push–push FET oscillator [1].

Both hybrid and monolithic MICs have planar transmission lines in common. Defining characteristics of transmission lines is essential for design of a microwave circuit, as they play key role in general performance of the circuit.

2.1 Transmission Lines

Any multiconducting structure that supports TEM or non-TEM modes of propagation is commonly referred as a "transmission line". In general transmission lines are characterized by following four basic parameters

1. $\mathbf{Z_0}$**:** characteristic impedance
2. $\mathbf{V_p}$: phase velocity
3. $\boldsymbol{\gamma}$ **:** propagation constant
    a. $\boldsymbol{\alpha}$: attenuation constant
    b. $\boldsymbol{\beta}$**:** phase constant
4. $\mathbf{P_{max}}$: peak power-handling capability

Besides to these electrical parameters, there are also some physical parameters which are helpful for characterization of transmission lines, like geometric cross section and conductor material used.

A uniform transmission line can be expressed with lumped series resistance (R_{un}), series inductance (L_{un}), shunt conductance (G_{un}), and shunt capacitance (C_{un}), all defined in per unit length of the line, as illustrated in Figure 2.3.

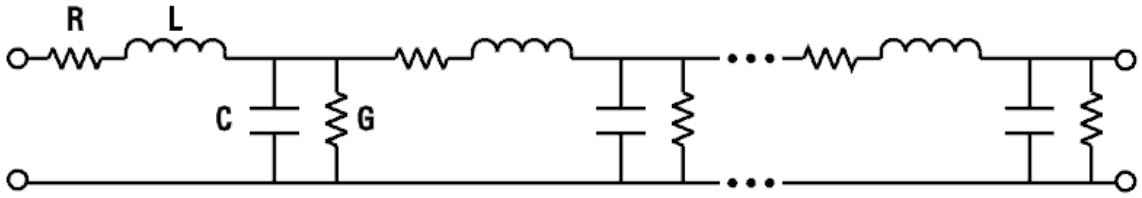


Figure 2. 3 Lumped circuit representation of a uniform transmission line

Propagation constant (ɣ), attenuation constant (α), phase constant (β), and characteristic impedance Z_0 are summarized in Table 2.1 [3].

Table 2. 1 Summary of fundamental expressions

Parameter	General Expression	Ideal Line	Low-Loss Line
Propagation constant ɣ =α+jβ	$\sqrt{(\overline{R}+jw\overline{L})+(\overline{G}+jw\overline{C})}$	$jw\sqrt{\overline{L}\overline{C}}$	$\left(\frac{\overline{R}}{2Z_0}+\frac{\overline{G}Z_0}{2}\right)+ jw\sqrt{\overline{L}\overline{C}}\left(1-\frac{\overline{R}\overline{G}}{4w^2\overline{L}\overline{C}}+\frac{\overline{G}^2}{8w^2\overline{C}^2}+\frac{\overline{R}^2}{8w^2\overline{L}^2}\right)$
Phase constant β	Im(ɣ)	$w\sqrt{\overline{L}\overline{C}}$ = $w/v_p = 2\pi/\lambda$	$w\sqrt{\overline{L}\overline{C}}\left(1-\frac{\overline{R}\overline{G}}{4w^2\overline{L}\overline{C}}+\frac{\overline{G}^2}{8w^2\overline{C}^2}+\frac{\overline{R}^2}{8w^2\overline{L}^2}\right)$
Attenuation constant α	Re(ɣ)	0	$\frac{\overline{R}}{2Z_0}+\frac{\overline{G}Z_0}{2}$

Characteristic impedance Z_0	$\sqrt{\frac{\overline{R}+jw\overline{L}}{\overline{G}+jw\overline{C}}}$	$\sqrt{\frac{\overline{L}}{\overline{C}}}$	$\sqrt{\frac{\overline{L}}{\overline{C}}}\left[1+j\left(\frac{\overline{G}}{2w\overline{C}}-\frac{\overline{R}}{2w\overline{L}}\right)\right]$

Transmission lines can be classified into two groups as conventional transmission structures, like coaxial line and waveguides, and planar transmission lines. For the sake of keeping the paper brief and getting down quickly to the components which were employed during the realization of the paper's circuit, I will not go over all transmission structures. Instead I will focus on planar transmission lines, in particular, on the microstrip lines.

2.1.1 Planar Transmission Lines

Planar transmission lines are important and essential components of most microwave circuits. They are used for various purposes depending on circuit's requirements. Baluns, filters, couplers, impedance matching circuits, and etc. can be realized by planar transmission lines.

Today lots different planar transmission lines exist; where some have been developed for special requirements. Each transmission line has its own unique advantages and disadvantages, depending on circuit types and targets wanted to be attained. Most common transmission lines are shown in Figure 2.4, and on Table 2.2 some rudimentary properties of transmission lines are summarized for a comparison [1], and [2].

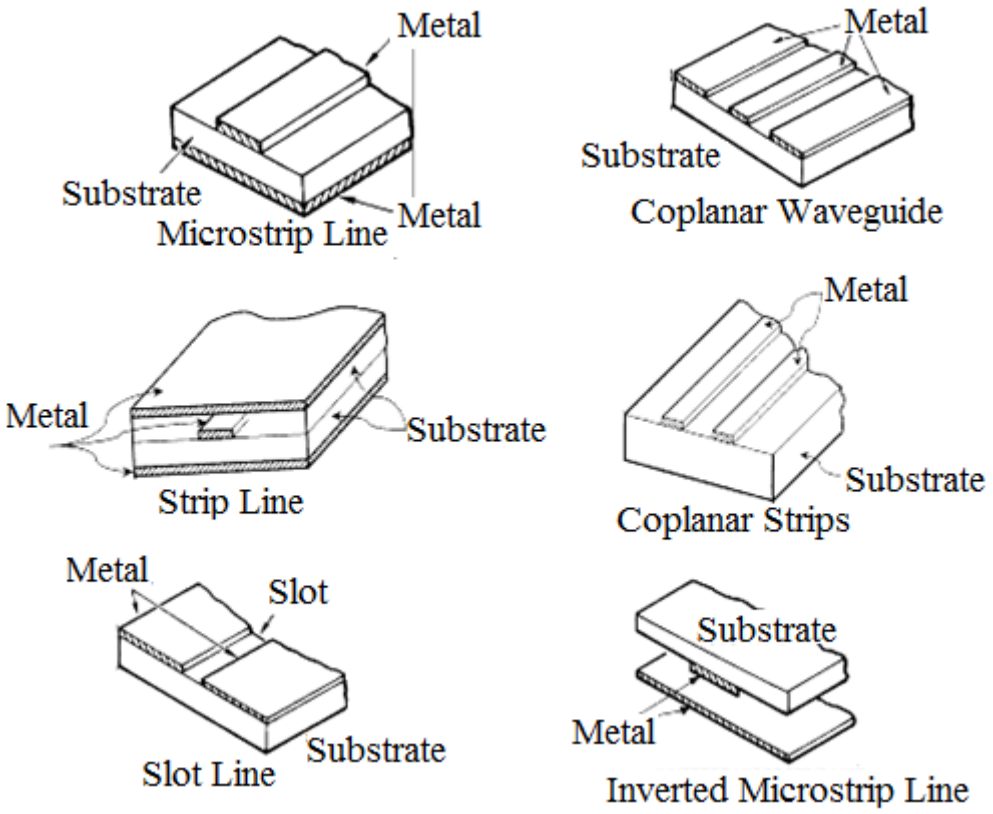


Figure 2. 4 The most common planar transmission lines. Most of planar lines have evolved from microstrip line and coplanar waveguide [3].

Table 2. 2 Characteristics of planar transmission lines.

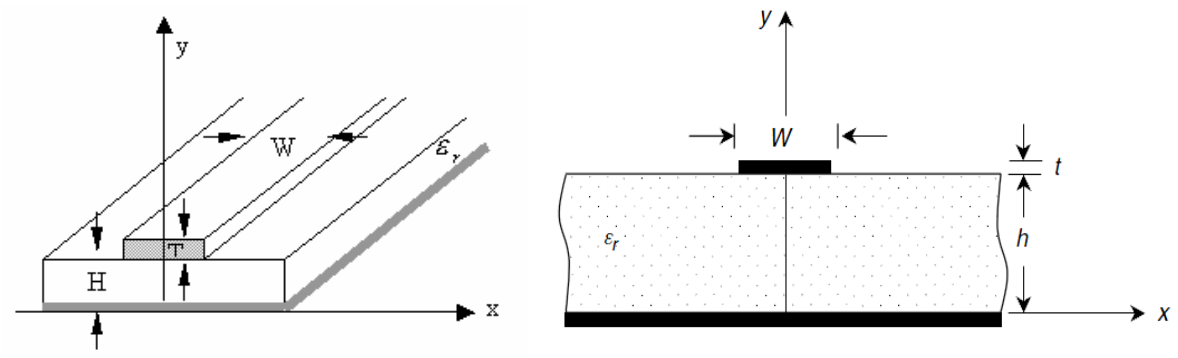
Type	Operating Frequency (GHZ)	Characteristic impedance range (Ohm)	Loss	Low-Cost Production
Microstrip line	≤ 110	10-100	High	Good
Coplanar waveguide	≤ 110	40-150	High	Good
Strip line	≤ 60	20-150	Low	Good
Coplanar strips	≤ 110	30-250	High	Good
Slot line	≤ 110	60-200	High	Good
Inverted microstrip line	≤ 220	25-130	Moderate	Fair

The distinct advantages of planar lines are light weight, small size, improved performance, relative low cost, reliability and reproducibility. As mentioned above there are great variety of planar transmission lines in use today. But I will discuss only microstrip planar transmission line, because the microstrip line was used during the realization of the circuit.

2.1.2 Microstrip Lines: *Open Microstrip Lines*

Microstrip line is the most popular and widespread planar transmission line due to its planar nature, easy fabrication, good mechanical support, good heat sinking, easy integration with solid-state devices, and abundance of design information.

Generally microstrip lines are obtained by placing conductor lines on upper surface of a substrate, which has a plate of conductor that is attached from the bottom to it. In Figure 2.5 top and cross-section views of a microstrip line is illustrated.



(a) (b)

Figure 2. 5 (a) Top view of microstrip line. (b) Cross section of a microstrip line.

Unlike the strip line, microstrip line is an inhomogeneous transmission line, since the field lines between the strip and the ground plane are not entirely encompassed in the substrate. This propagation mode is called as quasi-TEM. Thanks to image theory microstrip line can be expressed as two parallel plates which are placed at 2H distance in opposite directions, as shown in Figure 2.6 [2].

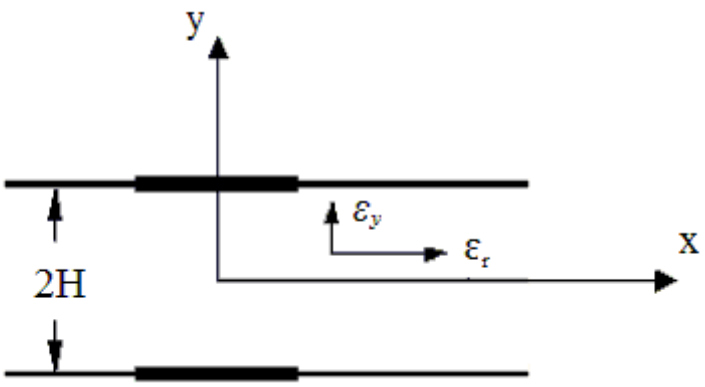


Figure 2. 6 Equivalent parallel-line circuit representation of a microstrip line [2].

During design of a MIC substrate properties, like dielectric constant, substrate thickness and conductor thinness, play vital role. Mostly, low-loss substrates are most desired, with very thin (negligible) metal conductor. In the Table 2.3 some common substrates with their properties are enlisted.

Table 2. 3 Common substrates in use

Semi-conducting Substrates	**ε_r horizontal sub. constant**	**ε_y vertical sub. constant**	**Tangent loss**	**Heat conductivity**
PTFE/woven glass	2.84	2.45	0.001-0.002	Low
PTFE/microfiber glass	2.26	2.2	0.0005-0.001	Low
RT/Duroid 5880	2.26	2.2	0.001	Low
Gallium Arsenic (GaAs)	12.9	12.9	0.0005-0.001	Medium
Silicon	11.7-12.9	11.7-12.9	0.001-0.003	Medium
Aluminum	9.6-10.1	9.6-10.1	0.005-0.002	Good

Even though that microstrip lines are simple to print and illustrate, it is very hard to precisely characterize their electrical behavior. Numerical methods prove themselves to be inconvenient and time-consuming requiring extensive calculations. Some closed-form equations have been

developed for fast calculation. These closed-form equations are extensively used in computer aided design (CAD) of microwave circuits. Here are closed-form equations of Z_0, ε_{ef}, and α:

Characteristic impedance

$$Z_0 = \begin{cases} \frac{\eta_0}{2\pi\sqrt{\varepsilon_e}} \ln\left(\frac{8h}{W'} + 0.25\frac{W'}{h}\right); if\ \frac{W}{h} \le 1 \\ \frac{\eta_0}{\sqrt{\varepsilon_e}}\left[\frac{W'}{h} + +1.393 + 0.667\ln\left(\frac{W'}{h} + 1.444\right)\right]^{-1}; if\ \frac{W}{h} \ge 1 \end{cases} \quad (2.1)$$

where

$$\eta_0 = 120\pi\ (\Omega) \quad (2.2)$$

$$\frac{W'}{h} = \frac{W}{h} + \frac{1.25}{\pi}\frac{t}{h}\left(1 + \ln\frac{4\pi W}{t}\right), \frac{W}{h} \le \frac{1}{2\pi} \quad (2.3)$$

$$\frac{W'}{h} = \frac{W}{h} + \frac{1.25}{\pi}\frac{t}{h}\left(1 + \ln\frac{2h}{t}\right), \frac{W}{h} \ge \frac{1}{2\pi} \quad (2.4)$$

Effective dielectric constant

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}F\left(\frac{W}{h}\right) - \frac{\varepsilon_r - 1}{4.6}\frac{t/h}{\sqrt{W/h}} \quad (2.5)$$

$$F\left(\frac{W}{h}\right) = \begin{cases} 1 + 12\frac{h}{W}^{-0.5} + 0.04\left(1 - \frac{W}{h}\right)^2, \frac{W}{h} \le 1 \\ 1 + 12\frac{h}{W}^{-0.5}, \frac{W}{h} \ge 1 \end{cases} \quad (2.6)$$

Attenuation constant (dB/unit length) $\alpha = \alpha_c + \alpha_d$ (2.7)

where

α_c: *conductivity loss*

α_d: *dielectric loss*

$$\alpha_c = \begin{cases} 1.38\dfrac{R_s}{hZ_0}\dfrac{32-\left(\dfrac{W'}{h}\right)^2}{32+\left(\dfrac{W'}{h}\right)^2}\Lambda, \dfrac{W}{h}\le 1 \\ 6.1\times 10^{-5}\dfrac{R_s\varepsilon_e Z_0}{h}\left(\dfrac{W'}{h}+\dfrac{0.667W'/h}{W'/h+1.444}\right)\Lambda, \dfrac{W}{h}\ge 1 \end{cases} \quad (2.8)$$

$$\alpha_d = 27.3\frac{\varepsilon_r}{\sqrt{\varepsilon_e}}\frac{\varepsilon_e-1}{\varepsilon_r-1}\frac{\tan\delta}{\lambda_0} \quad (2.9)$$

where tangent loss is

$$\tan\delta = \frac{\varepsilon''}{\varepsilon'} \approx \delta \quad (2.10)$$

Tangent loss is generated due to complex nature of dielectric losses

Dielectric loss: $\varepsilon = \varepsilon' - j\varepsilon''$ (2.11)

$$\Lambda = \begin{cases} 1+\left(\dfrac{W'}{h}\right)^{-1}\left(1+\dfrac{1.25t}{\pi W}+\dfrac{1.25}{\pi}\ln\dfrac{4\pi W}{t}\right), \dfrac{W}{h}\le\dfrac{1}{2\pi} \\ 1+\left(\dfrac{W'}{h}\right)^{-1}\left(1-\dfrac{1.25t}{\pi W}+\dfrac{1.25}{\pi}\ln\dfrac{2h}{t}\right), \dfrac{W}{h}\ge\dfrac{1}{2\pi} \end{cases} \quad (2.12)$$

2.2 Lumped Elements

A lumped element is a passive element whose size across any dimension is much smaller than the operating wavelength of the circuit or of wavelength to which upper frequency of bandwidth corresponds. It has to be so small, relative to the wavelength, that there is no

appreciable phase shift between the input and output terminals [4]. Today in the market there are lots of lumped elements on offer with different sizes and characteristics.

We can divide lumped elements basically into two classes, (a) ready-fabricated lumped elements; the ones with smallest dimensions are most commonly referred as chips-, and (b) on board printed lumped elements. In our circuit design we had to employed chip capacitors and indictors. Because of this I will briefly sketch over chip capacitors and inductor.

2.2.1 Chip Capacitors

Chip capacitors, as lumped elements, are extensively employed in MIC design, due to their low cost and easy soldering. In the market today, there are variety of chip capacitors with different sizes and dimensions. They are made by sandwiching high-dielectric-constant materials between parallel plates, as shown in Figure 2.7.

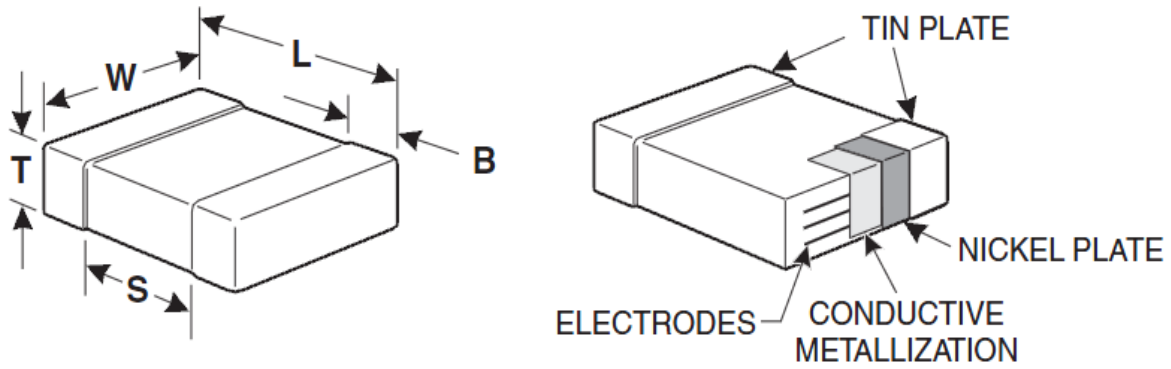


Figure 2. 7 A chip capacitor [4].

2.2.2 Chip Inductors

Inductors are widely used as circuit components in matching networks and biasing chokes. Below C-band frequencies, MICs using lumped inductors are an order of magnitude smaller than ICs using distributed matching elements such as microstrip lines or coplanar waveguides.

The width and thickness of the conductor determines the current-carrying capacity of the inductor. Thus, selecting a proper inductor becomes a vital issue as the inductor should allow bias current –which on its turn determines S parameters of transistors– pass through itself. In particular bias chokes used in power amplifier require high current capabilities.

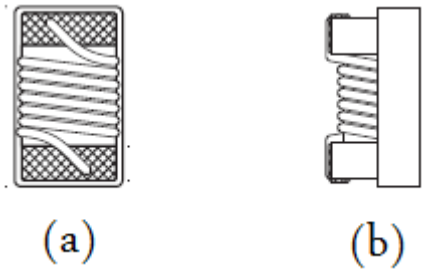


Figure 2. 8 A chip inductor. (a) Top view (b) Profile view

One of the most important parameter that should be taken to the consideration at very high frequencies is self-resonant frequency (SRF). The SRF (f_{res}) of an inductor is determined when $Im[Z_{in}]=0$; that is, the inductive reactance and the parasitic capacitive reactance become equal and opposite in sign. In other words, at this frequency the inductor functions more like resistor rather than an inductor. The inductor's first resonant frequency is of the parallel resonance type. Beyond the self-resonant frequency, the inductor is of capacitive nature. In general, value of the f_{res} is recommended to be three folds higher than operation frequency of the circuit [4]. For enhanced accuracy it is further advised to use S parameters at very high frequencies or at wavelength close to dimensions of the inductor or at relatively close frequencies to the f_{res}. S parameters of an inductor are generally provided by manufacturer.

2.3 Microwave Transistors

Any amplifier eventually has to contain at least one active device so that it could amplify the input signal. With advancement of technology lots of active state devices have been introduced to microwave industry. BJT, HBT, FET, HEMT and MESFETs enjoy an extensive use in microwave industry. Here I will not cover transistors in detail, because there is a colossal literature available which deals with transistors in depth, and for the sake of keeping

the paper content. Here, I will focus on basic concepts and fundamental characteristics that are helpful to characterize transistors in general.

2.3.1 Two-Port/N-Port Network Characterization: *S parameters*

Any given device or network -provided that it does not contain an independent source and satisfies the port conditions- can be represented either as a two-port network or as an N-port network, as illustrated in Figure 2.9.

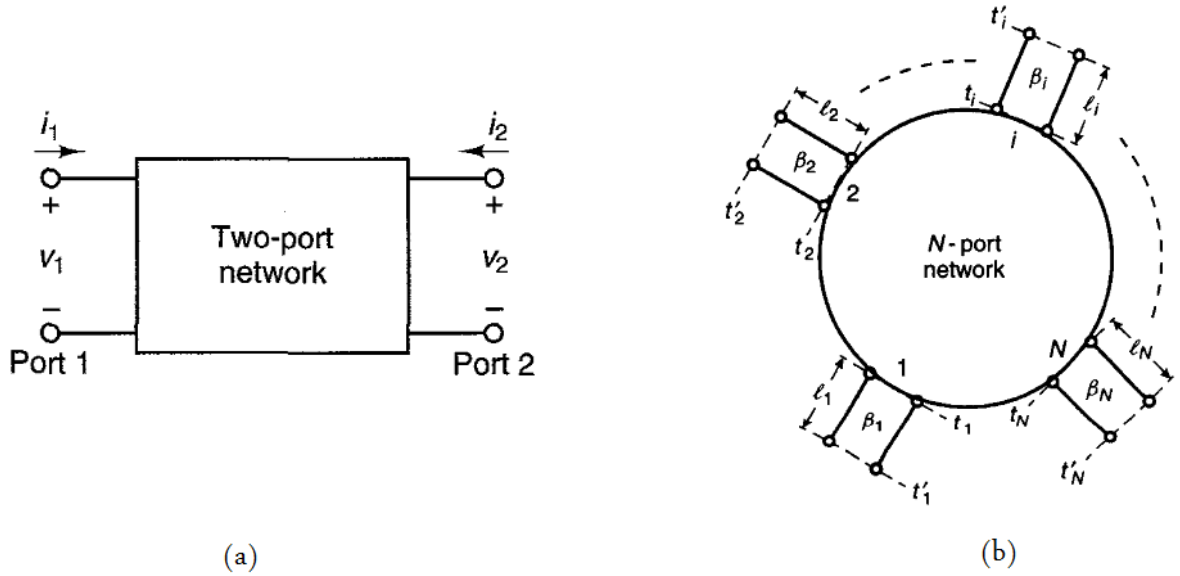


Figure 2. 9 (a) Two-port network (b) N-port network

Ports of a network must be parameterized in the way that it could represent inner-working of the network. At low frequencies, the *z*, *y*, *h*, or *ABCD* parameters are extensively used for representation of a network. But when it comes to very high frequencies waves start to scatter out of circuit making it difficult to test open and short circuit ends. To measure microwave in give range a proper termination is required.

A set of parameters that are very useful in microwave range is the *scattering parameters* (*S parameters*). These parameters are defined in terms of travelling waves and completely characterize the behavior of two-port networks, Figure 2.10. Definition and matrix form of S parameters for two and N-port networks are given in (2.13), (2.14), (2.15), (2.16), and (2.17).

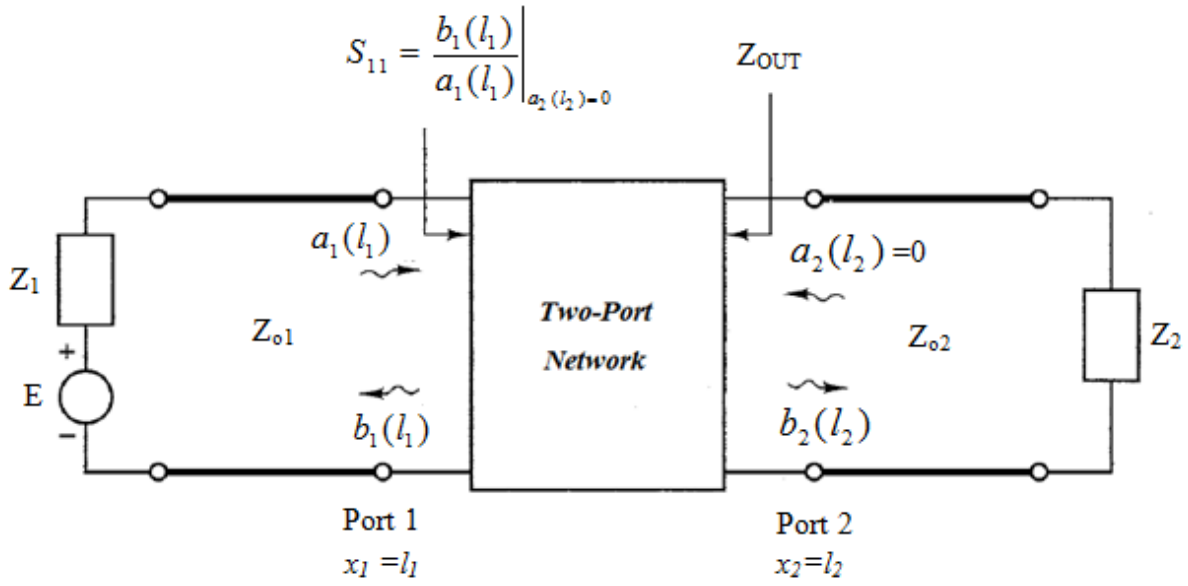


Figure 2. 10 Two-port network with sinusoidal voltage source with Z_1 source termination, Z_2 load termination, and with $a_{1,2}(x)$ and $b_{1,2}(x)$ travelling waves [15].

$$S_{11} = \left.\frac{b_1(l_1)}{a_1(l_1)}\right|_{a_2(l_2)=0} \quad S_{21} = \left.\frac{b_2(l_2)}{a_1(l_1)}\right|_{a_2(l_2)=0} \tag{2.13}$$

$$S_{12} = \left.\frac{b_1(l_1)}{a_2(l_2)}\right|_{a_1(l_1)=0} \quad S_{22} = \left.\frac{b_2(l_2)}{a_2(l_2)}\right|_{a_1(l_1)=0} \tag{2.14}$$

S_{11}: input reflection coefficient with output properly terminated

S_{21}: forward transmission coefficient with output properly terminated

S_{12}: reverse transmission coefficient with input properly terminated

S_{22}: output reflection coefficient with input properly terminated

$$\begin{pmatrix} b_1(l_1) \\ b_2(l_2) \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1(l_1) \\ a_2(l_2) \end{pmatrix} \tag{2.15}$$

$$S = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \tag{2.16}$$

for N-port network

$$S = \begin{pmatrix} S_{11} & \cdots & S_{1n} \\ \vdots & \ddots & \vdots \\ S_{n1} & \cdots & S_{nn} \end{pmatrix} \tag{2.17}$$

It can be easily seen from (2.13) and (2.14) that values of S parameters depend on reference plane. When it comes to a transistor, S parameters are measured under *small-signal conditions* at given biasing (Q) point, because S parameters alter at different Q points. In addition to that S parameters vary with frequency; therefore, S parameters are measured at several frequencies and are always included in or attached to a catalogue of the device by manufacturer. S parameters for different biasing conditions of NE3511S02 HJ-FET are presented in Table 2.4 and Table 2.5 as an example.

Table 2. 4 S parameters of NE3511S02 at V_{DS} = 2V and I_D=10mA

F	S11		S21		S12		S22	
GHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
2	0.97	-25.50	5.023	150.7	0.024	73.7	0.612	-18.5
2.5	0.948	-32.50	4.964	143.20	0.029	68.30	0.607	-22.30
3	0.930	-38.60	4.954	136.20	0.035	65.50	0.598	-27.10
3.5	0.912	-44.90	4.916	129.10	0.040	61.40	0.583	-31.70
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
18	0.496	93.50	2.997	-57.70	0.164	-24.00	0.239	140.20

Table 2. 5 S parameters of NE3511S02 at V_{DS} = 3V and I_D=20mA

F	S11		S21		S12		S22	
GHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
2	0.961	-26.80	5.997	149.00	0.022	73.10	0.586	-17.60
2.5	0.935	-34.00	5.902	141.10	0.025	71.30	0.580	-21.00

3	0.913	-40.30	5.853	133.80	0.031	67.00	0.573	-25.70
3.5	0.889	-46.80	5.772	126.50	0.036	63.30	0.558	-29.90
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
18	0.472	96.20	3.279	-56.30	0.171	-18.90	0.245	154.20

2.3.2 Power Gain

Power gain is main goal of any LNA circuit; else it is not an amplifier. The maximum gain which can be derived from a transistor depends on its fabrication and manufacture properties. Anything beyond of it is unrealizable. So the selection of a proper transistor is an utmost task which must be addressed with special care in an amplifier design. Depending on the transistor we optimize and make decisions concerning the circuit. There are several power definitions; the most common one is transducer gain (G_T).

Transducer power gain is defined as the ratio of power to the load (Z_L) to the power available from the source to the network.

$$G_T \triangleq \frac{P_L}{P_{avs}} \tag{2.18}$$

From [7] and [9] G_T can be expressed as following :

$$G_T = \frac{|S_{21}|^2 \ 1-|\Gamma_S|^2 \ 1-|\Gamma_L|^2}{|1-S_{11}\Gamma_S \ 1-S_{22}\Gamma_L \ -S_{12}S_{21}\Gamma_S\Gamma_L|^2} \tag{2.19}$$

or

$$G_T = \frac{4R_S R_L |z_{21}|^2}{|z_{11}+Z_S \ z_{22}+Z_L \ -z_{12}z_{21}|^2} \tag{2.20}$$

where

$$\Gamma_{L,S} = \frac{Z_{L,S} - Z_0}{Z_{L,S} + Z_0} \tag{2.21}$$

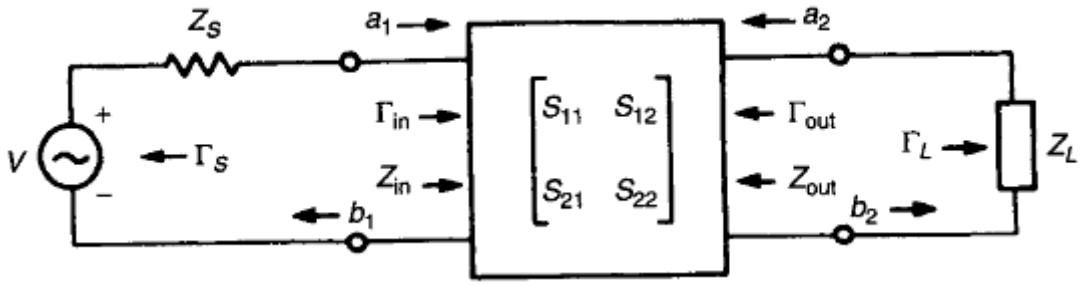


Figure 2. 11 Two port representation of a transistor amplifier [3].

2.3.3 Noise Figure

Each transistor generates it is own noise which has ill-effects on performance of the circuit. This noise is caused by random motion of electrons, and it is known as thermal or Johnson noise and expressed

$$N = kTB \tag{2.22}$$

where

N: maximum available noise power

k: Boltzmann's constant

B: noise bandwidth

As it is apparent from the (2.2) the thermal noise is not function of frequency, but bandwidth. Thus it cannot be filtered nor eliminated. This uniform distribution of noise among bandwidth is called as a white noise. The only thing that can be done with white noise is to accept it as it is and try to minimize its ill-effects.

The noise figure is defined as a ratio of signal-to-noise ratio at input to signal-to-noise ratio at output and expressed below:

$$NF \triangleq \frac{S_{in}/N_{in}}{S_{out}/N_{out}} = \frac{N_0}{GkTB} \tag{2.23}$$

where

N_0: available noise power at output

G: available gain power of network over bandwidth B

The overall noise figure of n cascaded networked is expressed at (2.24) where G_x is individual gain of the network and NF_x is individual noise figure of the network.

$$NF_{Total} = NF1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \frac{NF_4 - 1}{G_1 G_2 G_3} + \ldots + \frac{NF_n - 1}{G_1 G_2 G_3 \ldots G_n} \tag{2.24}$$

As it is evident from the (2.24) the noise and gain performance of the first network is the most important one. The noise of the first cascade has direct impact on the overall noise of a cascade network whereas gain has inverse impact. Because of this maximum gain and minimum noise are most desired parameters of first-stage LNA. Minimum noise figures are provided by manufacturers and available for several basing points at catalogs of transistors as shown in Table 2.6.

Table 2. 6 Noise parameters of NE425S01 hetero-junction FET at V_{DS} = 2 V, I_D = 10 mA biasing condition.

F (GHz)	NF_{min} (dB)	Γ_{opt}		$R_n/50$
		MAG.	ANG. (deg)	
2.0	0.31	0.93	14	0.38
4.0	0.34	0.80	29	0.33
6.0	0.40	0.65	48 0	0.25
8.0	0.45	0.49	72	0.18
10.0	0.52	0.36	102	0.11

⋮	⋮	⋮	⋮	⋮
18.0	1.00	0.47	–58	0.22

2.3.4 Biasing

Biasing a transistor at needed Q point is an important issue. As it was aforementioned, transistors' performance is dependent to Q points. For biasing the transistor at the Q point biasing circuit (network) has to be carefully designed. Biasing circuit is treated in detail in the third chapter.

CHAPTER 3

AMPLIFIER DESIGN: *Specifications and Optimization*

General Overview

An engineer of any discipline has to have clear and projected objective for any design. A microwave engineer is no exception. He has to clearly identify his target and know in detail methods that should be used for the design; and utterly, comprehend and embrace measurements that are used as figure of merit. In this chapter I will discuss main parameters that should be employed for a successful design of a low noise linear microwave amplifier.

The most important design considerations in a microwave transistor amplifier are stability, power gain, input and output VSWR –mismatch–, bandwidth, noise, and dc requirements, though there are many others. In our study we will refer our targets as a "required" and symbolize them as following:

NF_{req} *or* F_{req} *: required noise figure*

NF_{min} *or* F_{min} *: minimum noise figure*

G_{Treq} *: required transducer gain*

G_{Tmax} *: maximum transducer gain*

V_i *and* V_o *: input and out VSWR*

BW_{req} *: required bandwidth*

3.1 Mismatch and Matching Circuit

3.1.1 Maximum Power Transfer Theorem

In most cases attaining maximum power and making most of what is possible is the most desired feature of an electrical circuit. To understand what can be delivered to a load by source the "maximum power transfer theorem" was introduced.

Consider a load, with Z_L impedance, connected to an electrical source with internal impedance of Z_S, as shown in Figure 3.1.

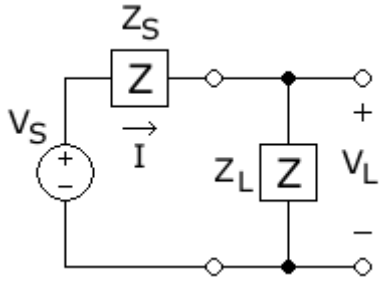


Figure 3. 1 A Z_L load connected to a Thevenin equivalent circuit.

The power delivered to the Z_L is

$$P_L \triangleq I_L \times V_L \tag{3.1}$$

where

I_L: current flowing through the load

V_L: voltage on two ends of the load

V_S: Source of Thevenin equivalent circuit

Hence, load's current can be express:

$$I_L = \frac{|V_S|}{|Z_S + Z_L|} \tag{3.2}$$

and from (3.2) the P_L can be rewritten as [9], [11]

$$P_L = I_{rms}^2 \times R_L = \frac{1}{2}\left|I_L^2\right| R_L = \frac{1}{2}\left[\frac{|V_S|}{|Z_S + Z_L|}\right] R_L = \frac{1}{2}\frac{|V_S|^2 R_L}{R_S + R_L{}^2 + X_S + X_L{}^2} \tag{3.3}$$

where

$$\text{Re } Z_S = R_S \; ; \; \text{Im } Z_S = X_S \tag{3.4}$$

$$\text{Re } Z_L = R_L \; ; \; \text{Im } Z_L = X_L \tag{3.5}$$

from (3.3)

$$P_L\Big|_{\left\{\begin{array}{c} R_S = R_L \\ X_S = -X_L \end{array}\right\}} = \frac{1}{8}\frac{|V_S|^2}{R_L} \tag{3.6}$$

which is the maximum power that can be delivered to the load. The (3.6) can concisely re-expressed with complex conjugate as:

$$P_L\Big|_{Z_S = Z_L^*} = P_{L_{\max}} = \frac{1}{8}\frac{|V_S|^2}{R_L} \tag{3.7}$$

At any given $Z_S \neq (Z_L)^*$, mismatch, power delivered to the load, P_L, will be equal to maximum power, P_{Lmax}. So without matching Z_S and Z_L no maximum power transfer can be attained. To deliver maximum power from source to the load you have to match Z_S to $(Z_L)^*$ or vice versa. The circuits that are used to satisfy this condition are called as "matching circuits".

3.1.2 Matching Circuits

Mismatch a big hurdle that has to be overcome if certain performance from circuit is expected. Impedance matching is important for maximum or required rate power transfer, improving the sensitivity of receivers, efficiency, and etc. There are many types of matching circuits which

meet particular requirements. Essentially, a matching circuit has to be properly selected/designed with following in mind (a) complexity, (b) bandwidth, (c) frequency response, and (d) ease of implementation. Figure 3.2 is a simple illustration of matching circuit which matches Z_1" to Z_2 .

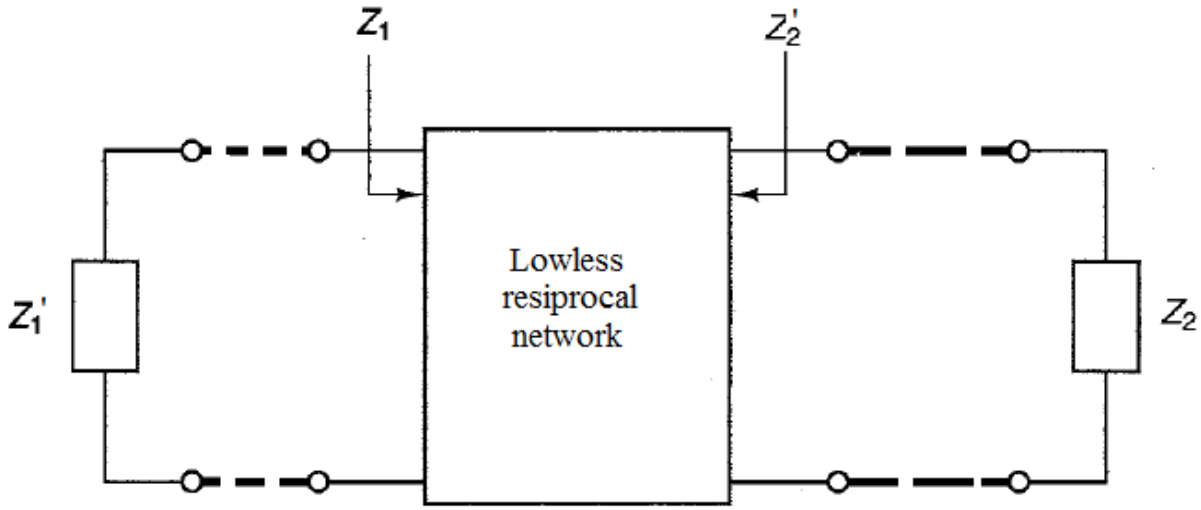


Figure 3. 2 Impedance transformation using matching circuit.

When it comes to a transistor you have to match both input and output ports of the amplifier to derive optimum power from the circuit.

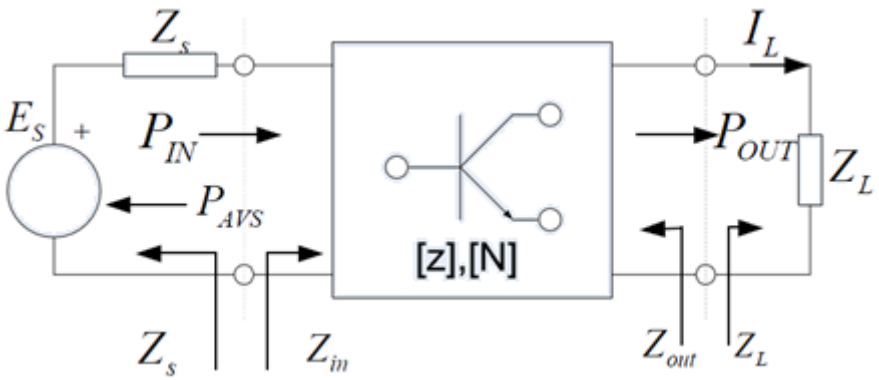


Figure 3. 3 An amplifier with no matching circuit.

In Figure 3.3 an amplifier with no matching circuit is illustrated. Thus the power delivered to the load is not equal to the maximum transferable power, $P_L \neq P_{Lmax.}$

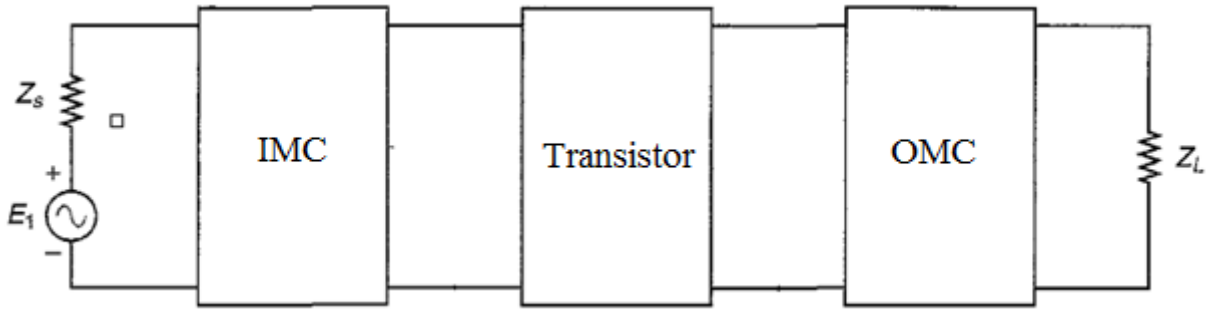


Figure 3. 4 Matched amplifier network. Both input and output ports ought to be matched [15].

Maximum available power can be delivered from E_1 to Z_L using input and output matching circuits, as shown in Figure 3.4. If a circuit is an N-stage cascade amplifier, then each stage's amplifier should be properly matched from both ports, as shown in Figure 3.5. Matching circuits can be easily calculated mathematically or found using Smith chart method in narrowband applications.

In microwave applications, depending on circuit and its operation frequency, lumped elements can be safely employed at matching circuits to some extent. But at very high frequencies distributed elements enjoy privilege over lumped elements. Moreover, ease of fabrication adds an extra plus to them. In general, L, T, and Π type matching circuits are employed as a matching circuit. But depending on circuit requirements, especially when high Q quality and wide bandwidth are of prime requirement, combination of L, T, and Π can be employed as a single matching network.

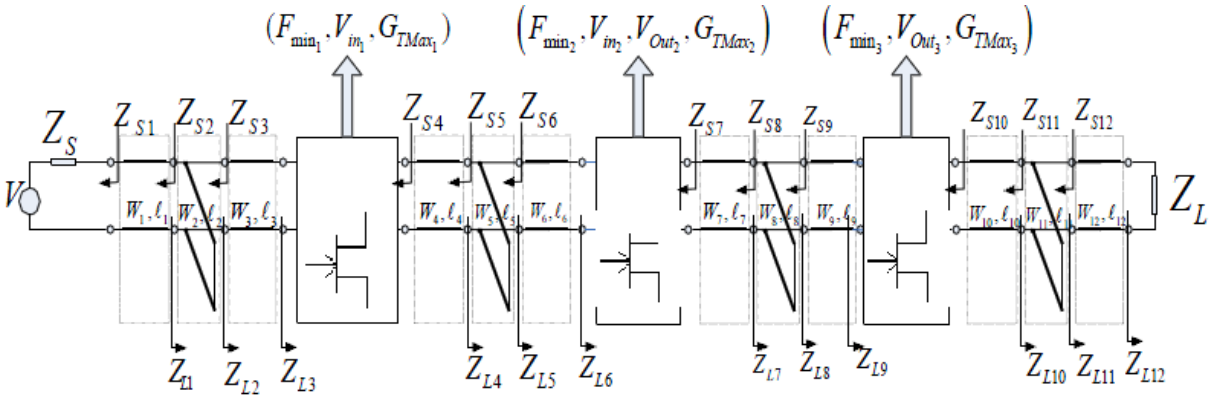


Figure 3. 5 Three-stage amplifier with T-T-T-T matching networks [2].

3.2 DC Biasing Network

DC biasing is an important part of an amplifier design. Holding a transistor at the desired quiescent point is achieved thanks to DC networks. The design considerations for biasing networks are efficiency, noise, oscillation suppression, RF chocking and impedance matching.

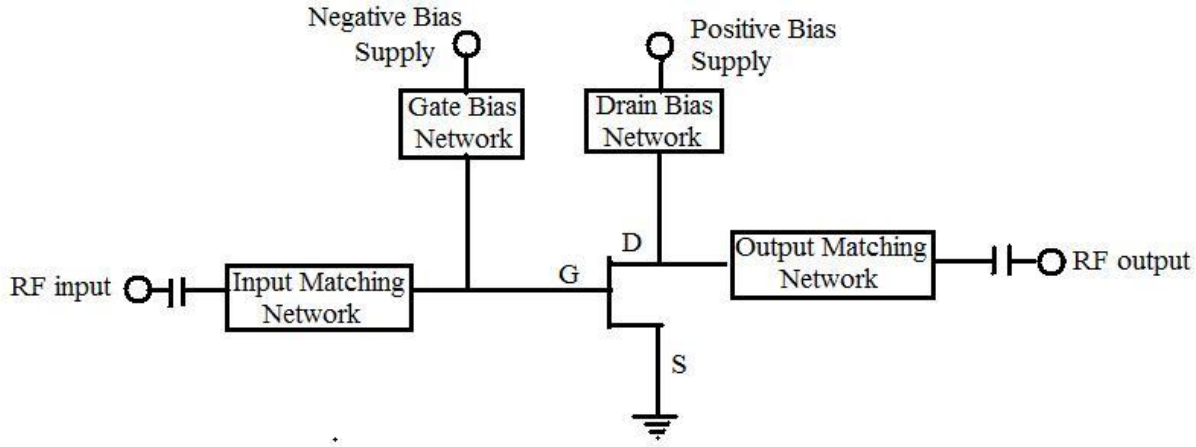


Figure 3. 6 Single-stage common source FET amplifier block diagram.

DC biasing networks can be classified in two types; (a) passive DC networks (b) active DC networks. Passive DC biasing circuit does not contain any active element, whereas active DC biasing circuit contains one or several active elements, like a transistor, as illustrated in Figure 3.7.

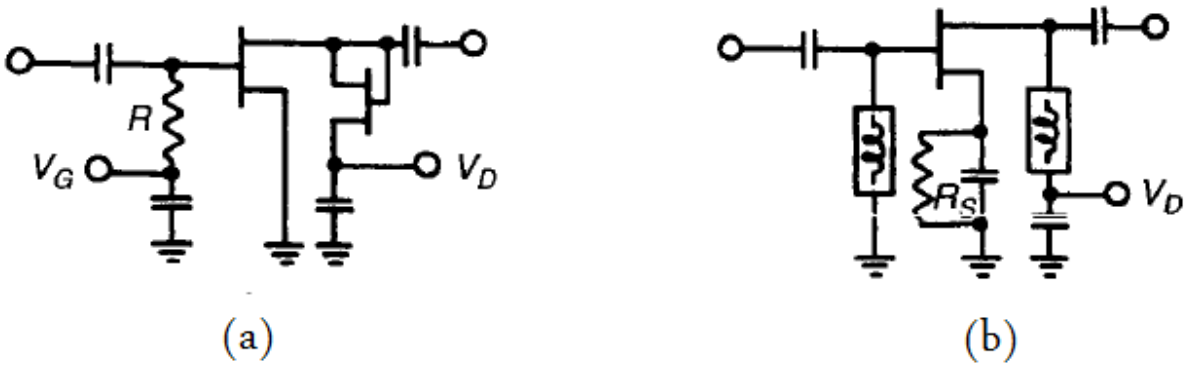
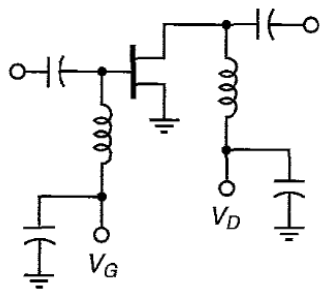
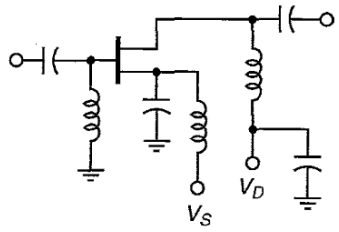
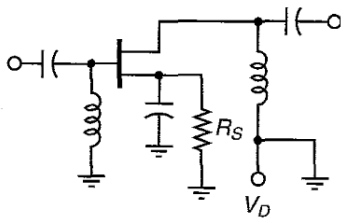
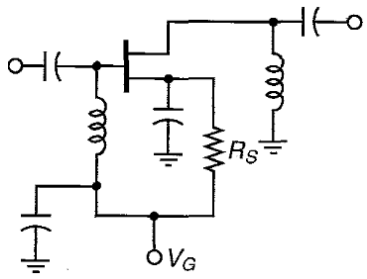


Figure 3. 7 DC biasing networks. (a) Active DC network with FET (b) Passive DC network

DC biasing circuit can be designed to have either one or two DC power supplies. An advantage of having two DC sources is that the source of a transistor is grounded with minimum possible source inductance, and hence, it can provide maximum gain. In Table 3.1 the most common DC circuits are illustrated with their characteristics.

Table 3. 1Most common DC bias networks [15].

Circuit	**How**	**Amplifier characteristics**	**Power supply used**
	Apply V_G, then V_D	Low noise, high power, high gain, high efficiency	Bipolar, minimum source inductance
	Apply V_S, then V_D	Low noise, high power, high gain, high efficiency	Positive supply
	Apply V_D	Low noise, high power, high gain, lower efficiency, gain easily adjusted by varying R_S	Unipolar
	Apply V_G	Low noise, high power, high gain, lower efficiency, gain easily adjusted by varying R_S	Negative unipolar

3.3 Grounding: Via Holes

Even though that grounding is very important theme in microwave circuits it is quite often ignored. Performance of a circuit can be optimized when the active device's ground path impedance is minimized. Here grounding is briefly sketched focusing on via holes as it was used during realization of the circuit.

Microstrip circuits are often mounted in housing to isolate them from other devices. Passive circuits such as filters that require only a single layer of microstrip can be grounded by directly attaching the microstrip substrate ground plane to the housing base.

Plated (via) holes -drilled through substrate- are extensively used to ground transmission lines and surface-mounted components such as amplifiers in microwave circuits. In practice, via hole's walls are either plated or filled completely with metal. A filled via has slightly lower DC resistance than a plated via. Primary advantage that a filled via enjoys over a plated via is its lower thermal resistance. When active components such as amplifiers must be mounted on top of a printed circuit, an array of filled vias under the active device provides a better thermal path than an array of plated vias [16].

Because each metal has its own resistance of metallization, via hole cannot be considered as a pure short circuit. Instead it can be roughly modeled as a series resistor and inductor, as shown in figure Figure 3.8.

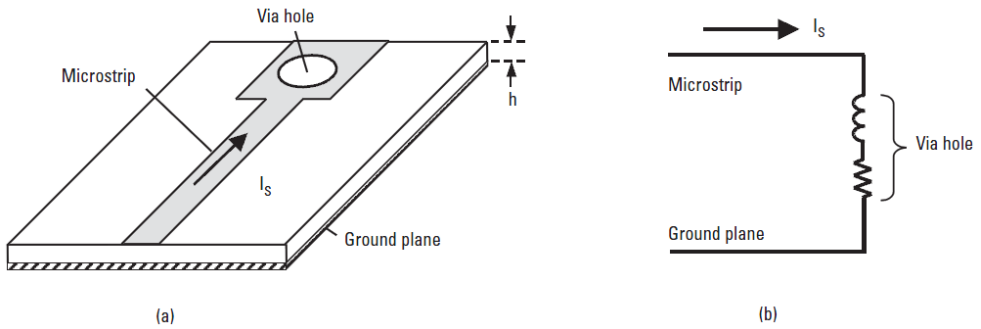


Figure 3. 8 (a) Current flow down through via hole to ground. (b) Equivalent circuit of via hole [16].

Resistor and inductor of a via hole can be expressed with following equations:

$$R_{via}\ \ f\ \ = R_{DC}\ \ 1+ f / f_{\delta}\ \ ^{1/2} \tag{3.8}$$

$$L_{via} = \frac{\mu_0}{2\pi}\left[h\ln\left(\frac{h+\sqrt{r^2+h^2}}{r} \right)+\frac{3}{2}\ \ r-\sqrt{r^2+h^2}\ \ \right] \tag{3.9}$$

where

$$R_{DC} = h\Big/\ \ \sigma\pi\left[r^2 -\ \ r-t\ \ ^2 \right] \tag{3.10}$$

$$f_{\delta} = 1\Big/\ \ \pi\mu_0\sigma t^2 \tag{3.11}$$

As seen from the 3.8 and 3.9 resistance and inductance increase in value as operation frequency increases. But resistance changes slightly relatively to inductance. Inductance increases and becomes more dominant at high frequencies forcing via holes to resemble less and less a short circuit. Hence, gain, noise, and other parameters of a transistor and circuit, in general, start to deteriorate significantly. Obviously, at very high frequencies grounding becomes more pressing issue than it is at low frequencies.

Impedance of a via hole can be decreased by two means. You can either reduce thickness of the substrate or drill a second via nearby the first one. Reducing substrate's thickness may not be always an option. Second via lowers the inductance to ground by about one-third.

3.4 Stability

Any amplifier may oscillate and generate unwanted outputs if treated with no care. Stability can be determined by the S parameters, the matching networks, and the terminations. In a two-port network, oscillation may occur either at input or output.

Oscillation, instability, occurs when either input or output port of a two-port network presents a negative resistance. This condition emerges when input or output reflection coefficient's

magnitude exceeds unit, and expressed in $|\Gamma_{IN}|>1$ or $|\Gamma_{OUT}|>1$. For a unilateral device it can be also said that negative resistance occurs when $|S_{11}|>1$ or $|S_{22}|>1$.

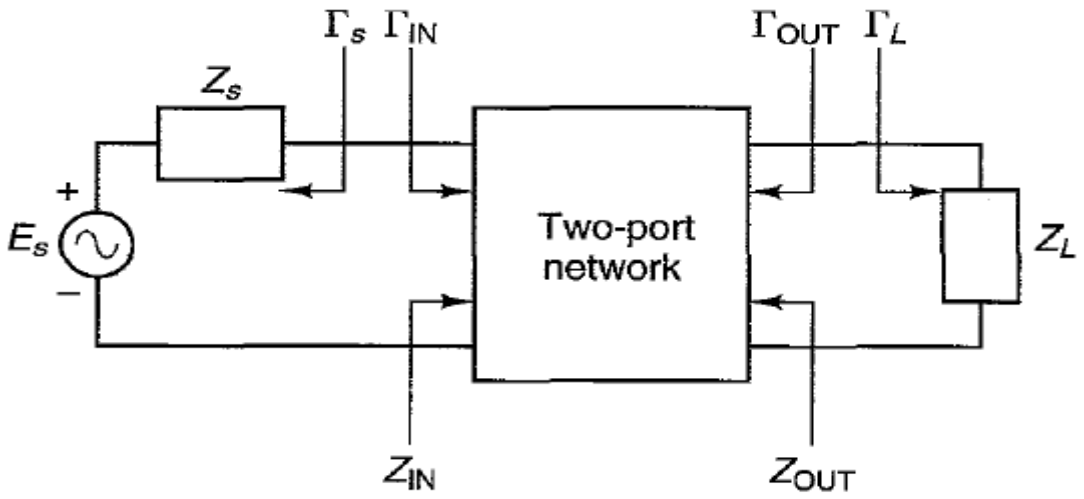


Figure 3. 9 Γ_{IN} and Γ_{OUT} representation for a two-port network.

Input reflection coefficient can be further expressed as a function of S parameter and reflection coefficient of the termination load, as shown in (3.14), and similarly, output reflection coefficient is a function of S parameter and reflection coefficient of source load, (3.15).

For unconditional stability at a given frequency following conditions must be met:

$$\left|\Gamma_S\right|<1 \tag{3.12}$$

$$\left|\Gamma_L\right|<1 \tag{3.13}$$

$$\left|\Gamma_{IN}\right| = f(S,\Gamma_L) = \left|S_{11}+\frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L}\right|<1 \tag{3.14}$$

and

$$\left|\Gamma_{OUT}\right| = g(S,\Gamma_S) = \left|S_{22}+\frac{S_{12}S_{21}\Gamma_S}{1-S_{11}\Gamma_S}\right|<1 \tag{3.15}$$

From (3.12), (3.13), (3.14), and (3.15) it can be easily understood that source load, termination load, and real parts of two-port network's input and output impedance must be positive. Since calculation of these equations is considerably cumbersome even at given single frequency, it becomes exhausting and time consuming, or even futile, effort at broadband designs. Thus, more sophisticated approaches are needed. For that "stability circles" approach has been developed [2], [13], and [12].

Since $\Gamma_{IN}=f(\Gamma_L)$, $\Gamma_{OUT}=g(\Gamma_S)$, their inverses $\Gamma_L=f^{-1}(\Gamma_{IN})$, $\Gamma_S=g^{-1}(\Gamma_{OUT})$ are linear fractional transformations, that they map circles in the related port and termination planes. Since $S_{12}S_{21}=0$, it follows:

$$\Gamma_L = f^{-1}(S, \Gamma_{IN}) = \frac{S_{11} - \Gamma_{IN}}{\Delta - S_{22}\Gamma_{IN}} \tag{3.16}$$

$$\Gamma_S = g^{-1}(S, \Gamma_{OUT}) = \frac{S_{22} - \Gamma_{OUT}}{\Delta - S_{11}\Gamma_{OUT}} \tag{3.17}$$

Using the transformations *f, g, f^{-1}*,and *g^{-1}* four different stability circles can be defined; and they are given in Table 3.2, where $\Delta=S_{11}S_{22}-S_{12}S_{21}$:

Table 3. 2 Stability circles

Stability circles in termination planes			
Original circle	**Mapped circle**	**Center point**	**Radius**
$\lvert\Gamma_{OUT}\rvert=1$	$g^{-1}(S, \lvert\Gamma_{OUT}\rvert=1)$ Source stability circle	$C_S = \frac{S_{11}^* - S_{22}\Delta^*}{\lvert S_{11}\rvert^2 - \lvert\Delta\rvert^2}$	$r_S = \left\lvert \frac{S_{12}S_{21}}{\lvert S_{11}\rvert^2 - \lvert\Delta\rvert^2} \right\rvert$
$\lvert\Gamma_{IN}\rvert=1$	$f^{-1}(S, \lvert\Gamma_{IN}\rvert=1)$ Load stability circle	$C_L = \frac{S_{22}^* - S_{11}\Delta^*}{\lvert S_{22}\rvert^2 - \lvert\Delta\rvert^2}$	$r_L = \left\lvert \frac{S_{12}S_{21}}{\lvert S_{22}\rvert^2 - \lvert\Delta\rvert^2} \right\rvert$

Stability circles in port planes			
Original circle	**Mapped circle**	**Center point**	**Radius**
$\left\|\Gamma_S\right\|=1$	$g(S,\left\|\Gamma_S\right\|=1)$ Output stability circle	$C_{OUT}=\frac{S_{22}-S_{11}^{*}\Delta}{1-\left\|S_{11}\right\|^2}$	$r_{OUT}=\left\|\frac{S_{12}S_{21}}{1-\left\|S_{11}\right\|^2}\right\|$
$\left\|\Gamma_L\right\|=1$	$f(S,\left\|\Gamma_L\right\|=1)$ Input stability circle	$C_{IN}=\frac{S_{11}-S_{22}^{*}\Delta}{1-\left\|S_{22}\right\|^2}$	$r_{IN}=\left\|\frac{S_{12}S_{21}}{1-\left\|S_{22}\right\|^2}\right\|$

Stability circles are meticulously researched by Prof. Dr. Filiz Güneş and her team in [12] and [13]. Because the stability consideration is a wide topic with huge literature available, I will not examine it in detail. After long calculations it can be found that for unconditional stability attaining following expressions is necessary and sufficient.

$$K=\frac{1-\left|S_{11}\right|^2-\left|S_{22}\right|^2+\left|\Delta\right|^2}{2\left|S_{12}S_{21}\right|}>1 \tag{3.18}$$

and

$$\left|\Delta\right|<1 \tag{3.19}$$

3.5 Computer Aided Design: *PSO optimization approach*

With advancement of computer technology engineers started to develop software that helped us quickly solve cumbersome equations, and microwave amplifier design is no exception. Today we have lots of software programs and tools which utilize variety of mathematical approaches, like gradient and boundary element methods. These methods are well known. The third prominent method of analysis is the Particle Swarm Optimization.

The particle swarm optimization method was introduced by J. Kennedy and R.C. Eberhart, in 1995. This is a method which imitates animal swarm movements and behaviors for optimization and finding global minimum and maximum peaks. PSO is a metaheuristic as it makes few or no assumptions about the problem being optimized and can search very large spaces of candidate solutions. PSO does not use the gradient of the problem being optimized, which means PSO does not require that the optimization problem be differentiable as is required by classic optimization methods such as gradient descent and quasi-Newton. PSO can therefore also be used on optimization problems that are partially irregular, noisy, change over time, and in particular non-linear equations.

Since PSO works with population of individuals randomly initialized, it should calculate each step's fitness, then update the swarm population accordingly after each fitness value, and at last stop its iteration when certain criteria(s) is/are met. However, there is neither crossover nor mutation operations, in PSO to update the population, only the best particles are used. For example, for an N-dimensional problem, the position and velocity can be specified by *MxN* matrix, where *M* is the number of particles in the swarm. Each row of the position matrix represents a possible solution to the optimization problem. The velocity of each particle depends on the distance of the current position to the positions that resulted in good fitness values. Each and every particle has to know its personal best and the global best position vectors for updating the velocity matrix after each iteration. Thus main goal a PSO algorithm is to update the matrix after each iteration of the algorithm. There are several types of PSOs, like repulsive PSO, asynchronous POs, and improved POS where each has its own unique specifications.

Asst. Prof. Dr. Salih Demirel has brilliantly shown in his [2] detailed work that PSO can be successfully employed for design of matching circuits for ultra-wideband amplifiers. In his work he had shown that PSO can solve complex requirements of amplifier network, like noise, bandwidth, input and output reflection, and gain. In [2] he had covered all possible combinations of matching circuits for single, two, and three-stage amplifiers. In my work I had employed PSO technic for design of matching circuits.

3.6 Design and Performance (F_{req}, V_{Ireq}, G_{Treq}) Triplets: *A geometrical approach*

An amplifier's behavior can be characterized with minimum four most essential functions: 'Transducer Gain (G_T)', Noise Figure (NF or F), input and output VSWR (V_i and V_{out}, respectively). And on its own turn, this triple function can be expressed with transistor's [z] parameters, termination load, and source load.

Any engineering application may either be constrained by well-proven mathematical formulations or physical possibilities. An amplifier design is also constrained by mainly following basic conditions:

$$F_{min} \leq F_{req};\ 1 \leq V_{Ireq};\ 1 \leq V_{OUTreq};\ G_{Tmin} \leq G_{Treq} \leq G_{Tmax} \tag{3.20}$$

and Z_{Sreq} and Z_{Lreq} must be a passive load that meets "unconditional stability" requirement of the circuit. Here, these characteristics are touched on in brief.

3.6.1 Required Noise Figure

Any transistor has its own internal noise. This internal noise cannot be filtered or eradicated; because of this it is called minimum noise. There is nothing to do to lower it down, but to content with it. Due to this fact any required noise figure for amplifier must be equal or larger than F_{min}, as expressed in (3.20), $F_{req}(Z_S, f|_{f0})$ is given by:

$$F_{REQ} \triangleq \frac{S_{in}/N_{in}}{S_{out}/N_{out}} = F_{MIN} + \frac{R_n}{|Z_{OPT}|^2}\frac{|Z_S - Z_{OPT}|^2}{R_S} \tag{3.21}$$

where R_n is equivalent noise resistor and $Z_{opt}=R_{opt}+jX_{opt}$ is optimum impedance of source load.

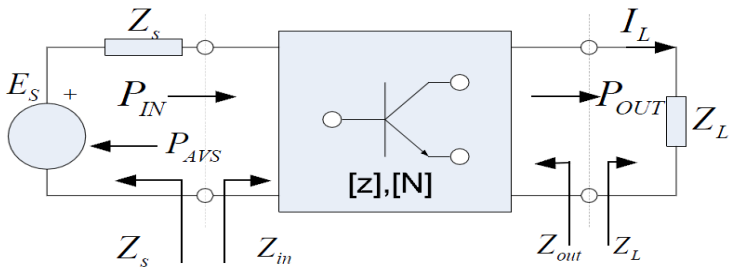


Figure 3. 10 Noise and Z parameter representation of a transistor

Constant noise circles can be derived from (3.21) for geometrical representation of F_{req} on Z_S plane.

$$\left|Z_S - Z_{OPT}\right|^2 = 2\mathrm{N}R_S \tag{3.22}$$

$$\left|Z_S\right|^2 - 2\ R_{OPT} + N\ R_S - 2X_C X_S + \left|Z_{OPT}\right|^2 = 0 \tag{3.23}$$

where $Z_{CN}=R_{CN}+jX_{CN}$ is a center point on Z_S plane and r_n is a radius of the circle;

$$R_{CN} = R_{OPT} + N \tag{3.24}$$

$$X_{CN} = X_{OPT} \tag{3.25}$$

$$r_n = \sqrt{N\ 2R_{OPT} + N} \tag{3.26}$$

$$\mathrm{N} = \frac{F_{REQ} - F_{MIN}}{2R_n}\left|Z_{OPT}\right|^2 \tag{3.27}$$

It can be easily seen from (3.24), (3.25), and (3.2), that the noise figure is represented by Z_{opt} phaser (dot) on Z_S plane if F_{req} is equal to F_{min} , and by a circle with finite radius if F_{req} is larger than F_{min}, as shown Figure 3.11

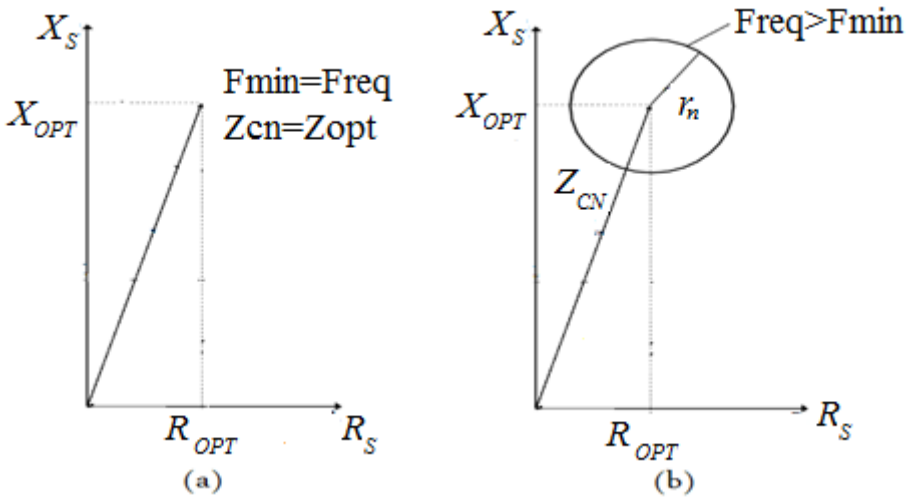


Figure 3. 11 (a) $F_{req} = F_{min}$; $r_n=0$ (b) Freq>Fmin; $r_n \neq 0$

3.6.2 Required Input VSWR

V_i is by definition:

$$\left|\rho_{in}\right| = \left|\frac{Z_S - Z_{IN}^*}{Z_S + Z_{IN}}\right| \tag{3.28}$$

Constant circle representation of Vi can be expressed as following by redistributing (3.28) in accordance to Z_S:

$$\left|Z_S\right|^2 - 2R_{IN}\frac{1+\left|\rho_{IN}\right|^2}{1-\left|\rho_{IN}\right|^2}R_S + 2X_{IN}X_S + \left|Z_{IN}\right|^2 = 0 \tag{3.29}$$

where, ρ is a reflection coefficient, Z_{IN} is an input impedance, Z_{cv} is center point of input VSWR circles at Z_S plane, and r_v is a radius of the circles:

$$Z_{vp} = R_{vp} + jX_{vp} = \frac{1+\left|\rho_{IN}\right|^2}{1-\left|\rho_{IN}\right|^2}R_{IN} + j(-X_{IN}); \tag{3.30}$$

$$r_v = \frac{2\left|\rho_{IN}\right|}{1-\left|\rho_{IN}\right|^2}R_{IN} \tag{3.31}$$

$$Z_{IN} = R_{IN} + jX_{IN} \tag{3.32}$$

From (3.30) and (3.31) it can be seen that when there is no reflection ($\rho_{in}=0 \leftrightarrow$ VSWR=1) the radius of the circle becomes zero and $R_{vp}=R_{IN}$.

3.6.3 Required Transducer Gain

Constant circle representation of a transducer gain can be expressed as following:

$$G_T \triangleq \frac{P_{OUT}}{P_{AVS}} = \frac{P_{IN}}{P_{AVS}} \frac{P_{OUT}}{P_{IN}} = \frac{4R_S R_L \left|z_{21}\right|^2}{\left| z_{11} + Z_S \quad z_{22} + Z_{L} \quad - z_{12} z_{21} \right|^2} \tag{3.33}$$

By redistributing (3.33) in accordance to Z_S we will get:

$$\left|Z_S\right|^2 - 2\left(\frac{C}{G_T} - R_{IN}\right) R_S - 2X_{IN} X_S + \left|Z_{IN}\right|^2 = 0 \tag{3.34}$$

where, C is a constant, Z_{cp} is center point of transducer gain circles at Z_S plane, and r_p is a radius of the circles:

$$C = \frac{2R_L \left|z_{21}\right|}{\left|Z_L + z_{22}\right|^2} \tag{3.35}$$

$$Z_{cp} = R_{cp} + jX_{cp} = \left(\frac{C}{G_T} - R_{IN}\right) + j(-X_{IN})\,; \tag{3.36}$$

$$r_p = \sqrt{\frac{C}{G_T}\left(\frac{C}{G_T} - 2R_{IN}\right)} \tag{3.37}$$

since

$$\frac{P_{IN}}{P_{AVS}} = \frac{\left|Z_S + Z_{IN}\right|^2 - \left|Z_S + Z_{IN}^*\right|^2}{\left|Z_S + Z_{IN}\right|^2} = \frac{4R_s R_{IN}}{\left|Z_S + Z_{IN}\right|^2} = 1 - \left|\rho_{in}\right|^2 \tag{3.38}$$

(3.33) can be re-expressed by using (3.38) for a given input VSWR as:

$$G_T = \frac{\left|z_{21}\right|^2}{\left|z_{22} + Z_L\right|^2} \frac{R_L}{R_{IN}} \left(1 - \left|\rho_{IN}\right|^2\right) \tag{3.39}$$

From the equations mention above we can confidently say that noise figure's and input VSWR's circles are enough for finding a solution, in terms of geometric approach it means that there is a solution for given F_{req} and Vi_{req} when a noise circle crosses input VSWR circle at least at one point.

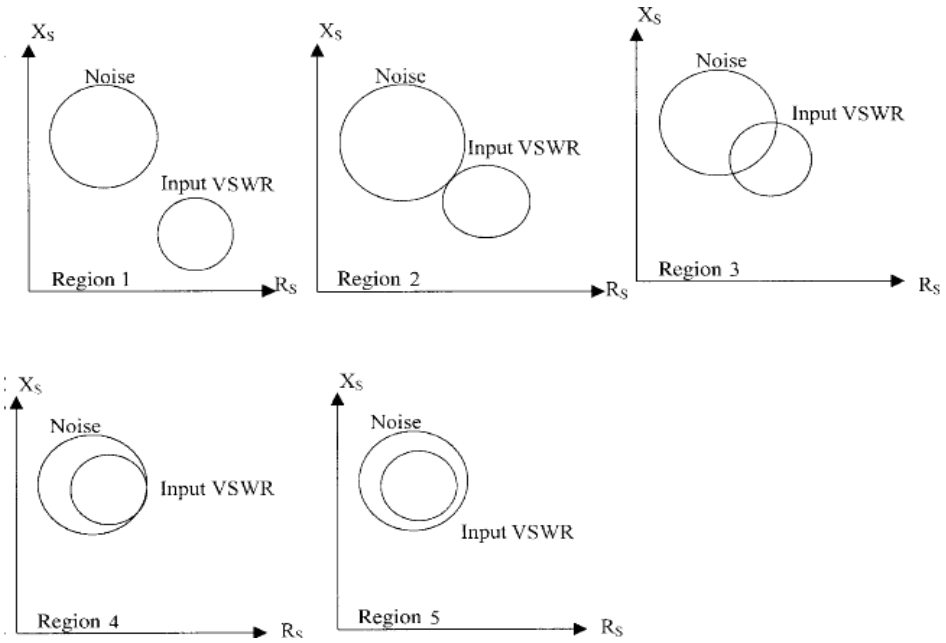


Figure 3. 12 The positions of the input VSWR circles with respect to the noise circle in the Z_S plane [7].

In first and fifth regions of Figure 3.12 circles do not cross. Thus there is no maximum G_T gain that could meet given noise and input requirements.

CHAPTER 4

SIMULATIONS and REALIZATION

In this chapter I will treat simulation and realization of my circuit.

4.1 A Transistor Selection

As it was mentioned in second chapter the selection of a proper transistor is very important. For that I had devoted this subheading to the selection of a transistor.

In the market today there are a lot of transistors available from variety of manufacturers, like Renesas Technology, ROHM, Vishay, and etc. In the first place we had eliminated transistors biasing on their operation bandwidth. The transistors which were selected are operable from C to Ku band. I had examined lots different transistors like, ATF36077, FHX13LG, NE3503M04, NE3511S02, NE3512S02, and etc. But for consistency of the paper and demonstration of main points I will focus on FHX13LG and NE3503M04.

4.1.1 FHX13LG

FHX13LG Super Low Noise HEMT can be characterized for V_{DS}=2V and I_{DS}=10mA with Figure 4.1and Table 4.1.

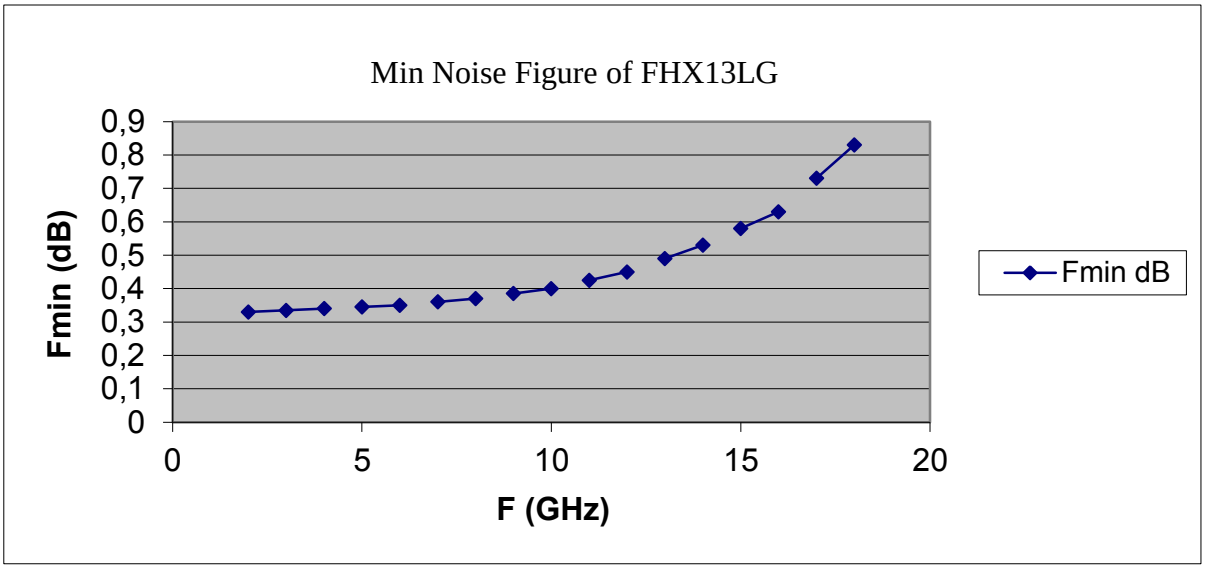


Figure 4. 1 Noise figure of FHX13LG at V_{DS}=2V, I_{DS}=10mA

Table 4. 1 S parameters of FHX13LG at V_{DS}=2V, I_{DS}=10mA

F	S11		S21		S12		S22	
GHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
4	0.862	-75.50	4.534	105.9	0.048	39.0	0.522	-62.0
5	0.811	-91.60	4.213	89.70	0.053	29.3	0.502	-75.6
6	0.763 -	-107.1	3.886	74.4	0.056	21.0	0.488	-89.6
7	0.727	-121.1	3.582	60.0	0.057	13.2	0.487	-103.0
8	0.701	-133.3	3.300	46.4	0.056	7.9	0.498	-114.9
9	0.682	-144.1	3.078	33.8	0.055	3.5	0.515	-125.0
10	0.659	-154.2	2.899	21.4	0.055	-0.0	0.531	-134.
11	0.636	-164.4	2.748	9.3	0.054	-2.6	0.544	-144.0
12	0.618	-175.4	2.593	-3.3	0.054	-5.2	0.561	-155.1
13	0.608	175.5	2.466	-14.8	0.054	-5.7	0.590	-164.0
14	0.596	166.6	2.366	-26.6	0.055	-7.8	0.619	-172.4
15	0.585	158.3	2.279	-38.3	0.056	-9.7	0.654	-179.7
16	0.564	148.8	2.244	-50.7	0.058	-12.8	0.677	172.6
17	0.543	138.2	2.217	-63.6	0.061	-17.6	0.701	163.4
18	0.525	127.3	2.185	-77.1	0.063	-24.7	0.727	154.1

The transistor was scrutinized for following three conditions;

a) $F_{MIN}=F_{REQ}$; $G_T=G_{Tmax}$; V_i =1.0;
b) $F_{MIN}=F_{REQ}$; $G_T=G_{Tmax}$; V_i =1.2;
c) $F_{MIN}=F_{REQ}$; $G_T=G_{Tmax}$; V_i =1.5;

Table 4. 2 Required source and termination loads for attaining maximum transducer gain, minimum noise figure and V_i=1

F (GHz)	V_{ireq}	F_{req}	G_{Tmax}	$Re(Z_{Lreq})$	$Im(Z_{Lreq})$	$Re(Z_{Sreq})$	$Im(Z_{Sreq})$
8	1	0,37	16,69836	-36,9765	-5,48248	9,009863	36,2159
9	1	0,385	15,82961	-30,749	-5,71003	9,650562	29,21465
10	1	0,4	15,03918	-25,8684	-8,31286	10,34101	23,01229
11	1	0,425	14,1036	-25,9542	-11,049	11,56872	17,57182
12	1	0,45	13,48091	-26,378	-13,464	12,92693	12,55841
13	1	0,49	13,28346	-28,0896	-14,2533	14,75868	8,484165
14	1	0,53	13,21649	-30,8222	-13,944	16,83012	4,665573
15	1	0,58	13,41573	-14,2498	3,324755	127,902	-8,52089
16	1	0,63	13,62199	-31,9998	-8,49543	22,49793	-1,74173
17	1	0,73	14,33993	-29,3203	-7,955	26,54545	-3,78565
18	1	0,83	66,48751	-	-	-	-

Table 4. 3 Required source and termination loads for attaining maximum transducer gain, minimum noise figure and V_i=1.2

F (GHz)	V_{ireq}	F_{req}	G_{Tmax}	$Re(Z_{Lreq})$	$Im(Z_{Lreq})$	$Re(Z_{Sreq})$	$Im(Z_{Sreq})$
8	1,2	0,37	13,84898	-38,25	-32,4177	9,009863	36,2159
9	1,2	0,385	11,28558	-25,0627	-34,2178	9,650562	29,21465
10	1,2	0,4	5,400344	-7,65094	-35,3427	10,34101	23,01229
11	1,2	0,425	2,848537	5,977057	-39,0079	11,56872	17,57182
12	1,2	0,45	6,145444	16,26855	-39,5901	12,92693	12,55841

13	1,2	0,49	7,126612	26,34043	-39,2971	14,75868	8,484165
14	1,2	0,53	7,368635	38,12127	-38,754	16,83012	4,665573
15	1,2	0,58	20,53914	-15,7737	4,760752	127,902	-8,52089
16	1,2	0,63	6,179366	81,3674	-31,9777	22,49793	-1,74173
17	1,2	0,73	3,421164	170,0794	12,85024	26,54545	-3,78565
18	1,2	0,83	-7,78323	9,550178	136,0228	31,17538	-5,16963

Table 4. 4 Required source and termination loads for attaining maximum transducer gain, minimum noise figure and V_i=1.5

F (GHz)	V_{ireq}	F_{req}	G_{Tmax}	$Re(Z_{Lreq})$	$Im(Z_{Lreq})$	$Re(Z_{Sreq})$	$Im(Z_{Sreq})$
8	1,5	0,37	1,881292	-6,01895	-60,2693	9,009863	36,2159
9	1,5	0,385	6,56103	15,90569	-42,1102	9,650562	29,21465
10	1,5	0,4	9,90942	24,55237	-18,975	10,34101	23,01229
11	1,5	0,425	10,87029	25,17553	-6,8071	11,56872	17,57182
12	1,5	0,45	10,976737	22,10299	-3,09663	12,92693	12,55841
13	1,5	0,49	10,986222	19,70414	-2,21203	14,75868	8,484165
14	1,5	0,53	10,885556	18,50511	-3,08523	16,83012	4,665573
15	1,5	0,58	17,800041	-17,3265	6,55603	127,902	-8,52089
16	1,5	0,63	10,442461	19,80637	-6,10454	22,49793	-1,74173
17	1,5	0,73	9,847715	24,17719	-8,15583	26,54545	-3,78565
18	1,5	0,83	9,123336	29,03439	-6,88789	31,17538	-5,16963

From Table 4.2, Table 4.3, and Table 4.4 Figure 4.2 and Figure 4.3 can be drawn:

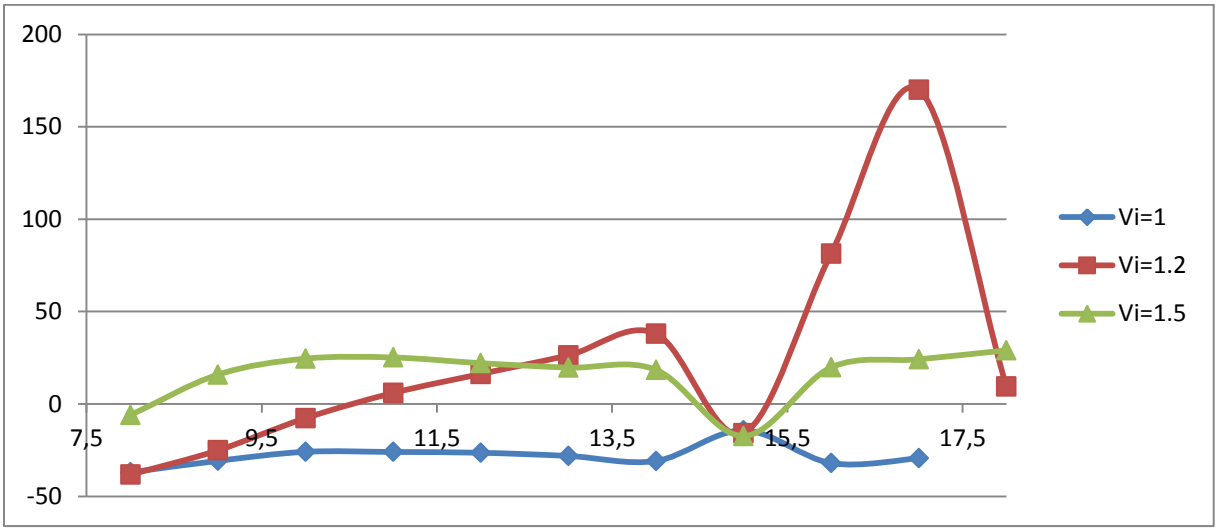


Figure 4. 2 Re{Z_{Lreq}} variation over bandwidth at given V_i values

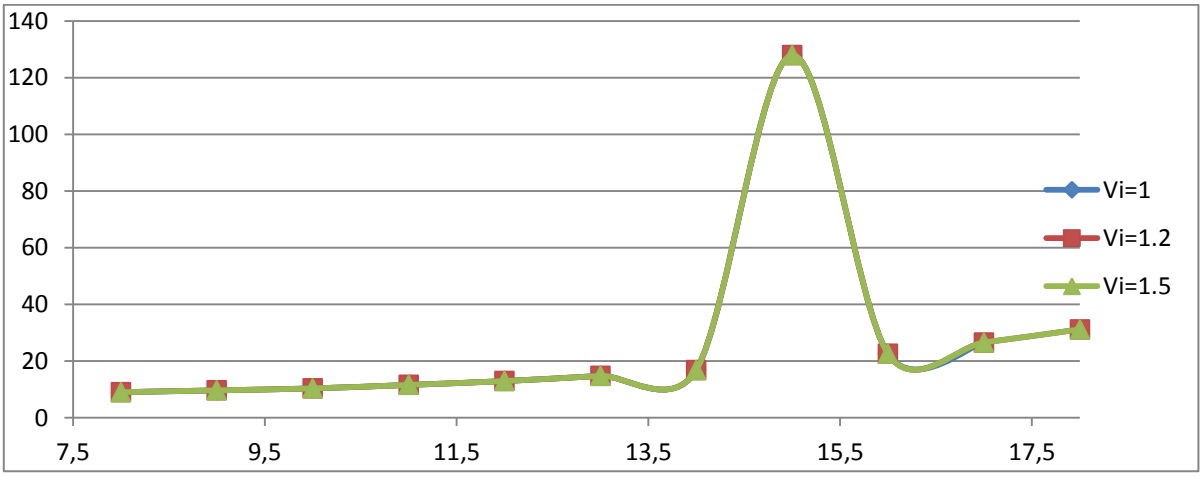


Figure 4. 3 Re{Z_{Sreq}} variation over bandwidth at given V_i values

It can be seen from Figure 4.2 that the Re{Z_{Lreq}} has negative values. As it was aforementioned, network becomes unstable at those points. Because of instability this transistor, FH X13LG, was dropped from the research.

Besides to FHX13LG I had examined several other transistors. But to get down directly to the results and circuit realized I will just focus on NE3503M04.

4.1.2 NE3503M04

NE3503M04, super low noise N-channel HJ-FET, was examined for different quiescent points like {V_{DS}=2V|I_{DS}=7mA}, {V_{DS}=2V|I_{DS}=10mA}, {V_{DS}=2V|I_{DS}=15mA}, {V_{DS}=3V|I_{DS}=10mA}, and so on. The best bandwidth and gain figures for given V_i were found for {V_{DS}=2V|I_{DS}=15mA}, as shown in Figure 4.3, Figure 4.4, Figure 4.5, and Figure 4.6.

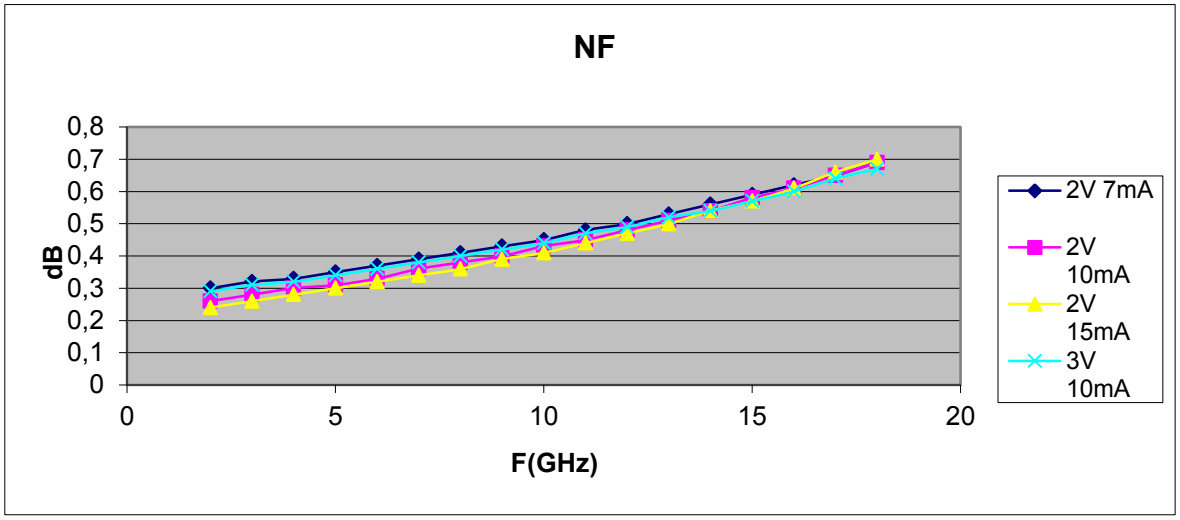


Figure 4. 4 Noise variation at different quiescent points

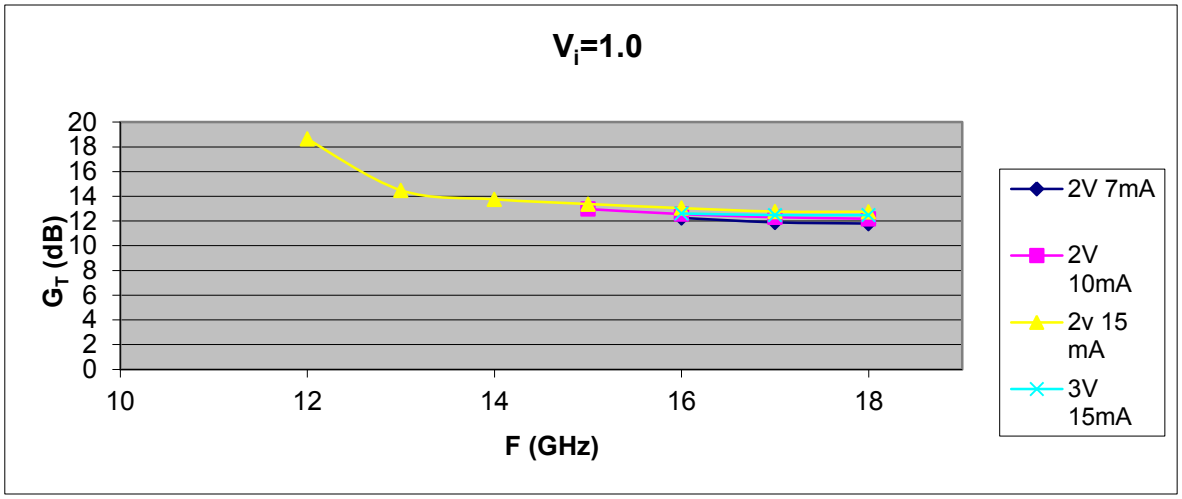


Figure 4. 5 Gain variation over bandwidth at V_i=1 and different quiescent points

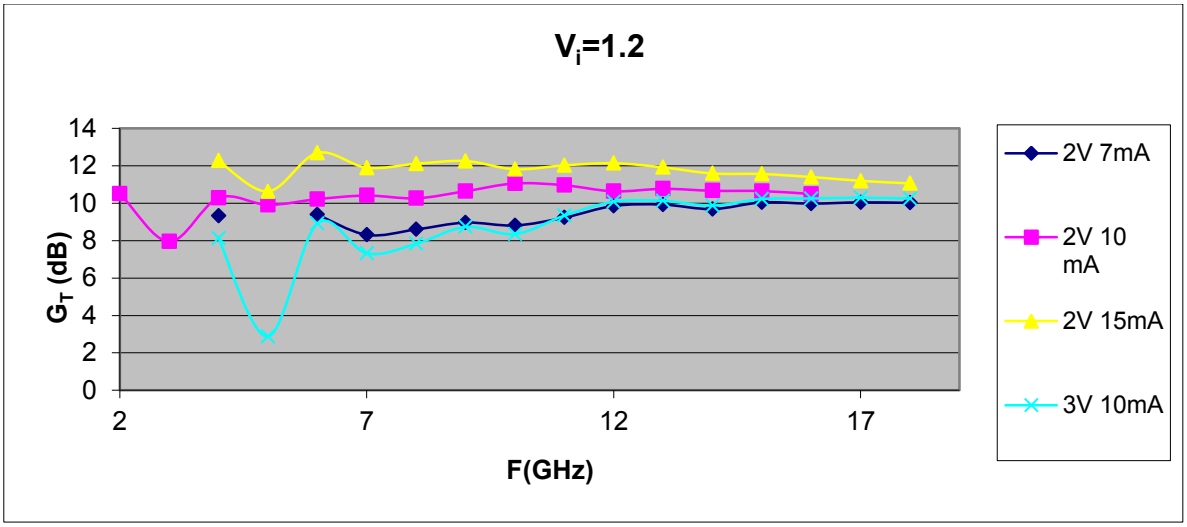


Figure 4. 6 Gain variation over bandwidth at V_i=1,2 and different quiescent points

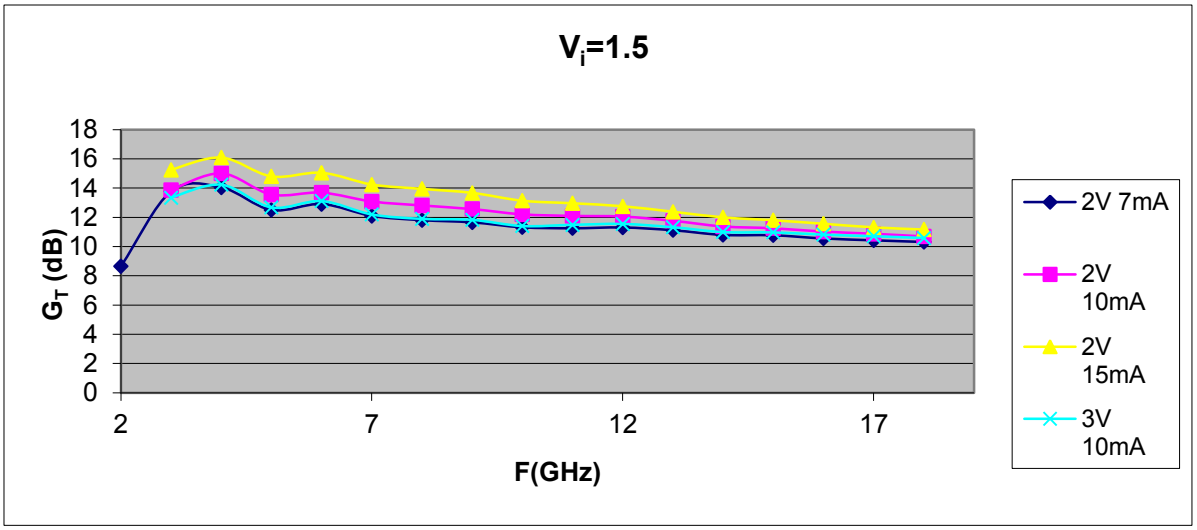


Figure 4. 7 Gain variation over bandwidth at V_i=1,5 and different quiescent points

Required source and load terminations are illustrated at Figure 4.7, Figure 4.8, Figure 4.9, and Figure 4.10 for given V_i value from 2GHz to 18GHz.

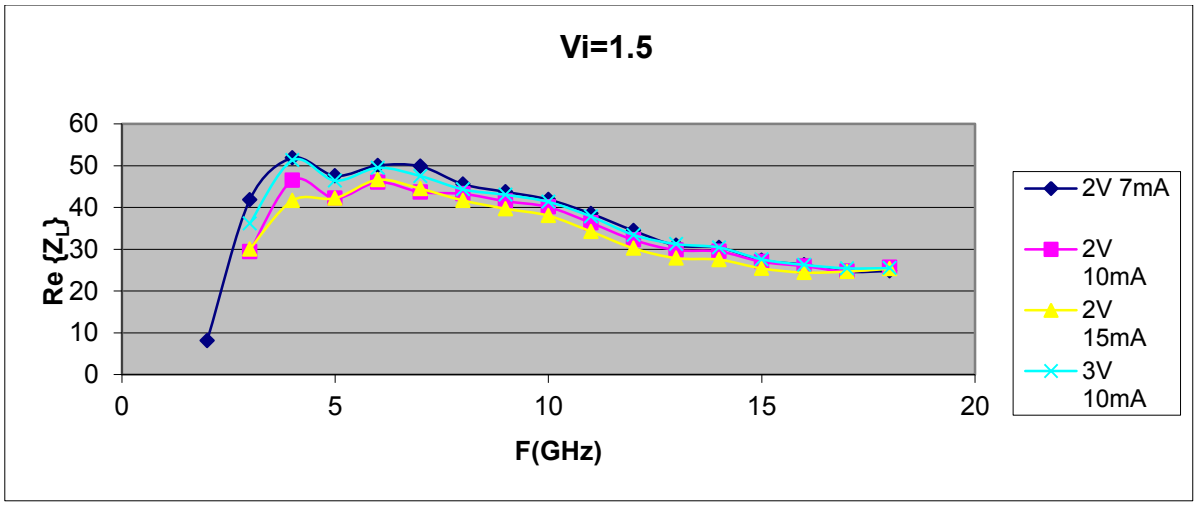


Figure 4. 8 Re{Z_L} variation over bandwidth at V_i=1,5 and different quiescent points

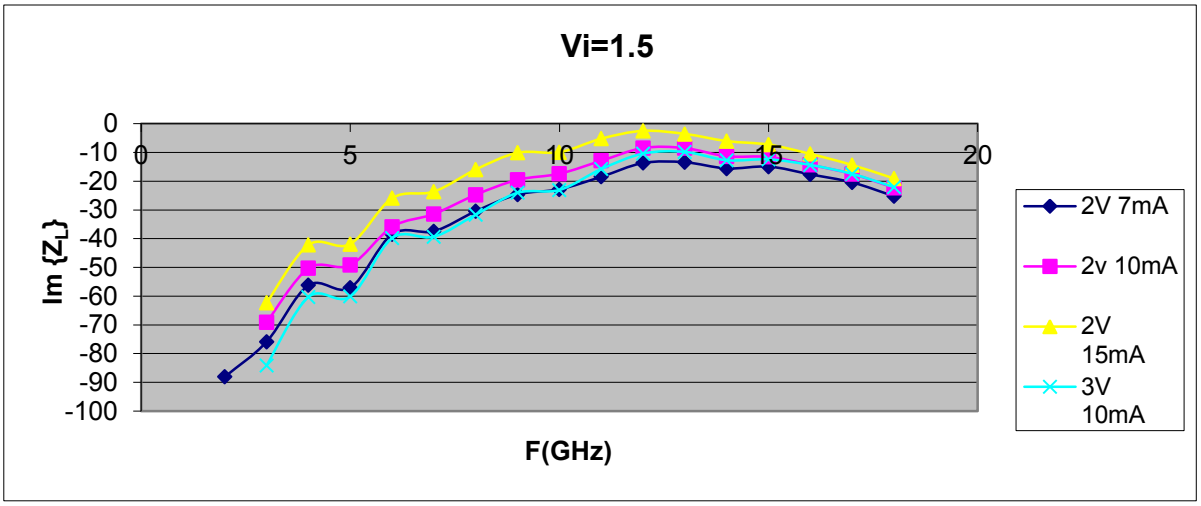


Figure 4. 9 Im{Z_L} variation over bandwidth at V_i=1,5 and different quiescent points

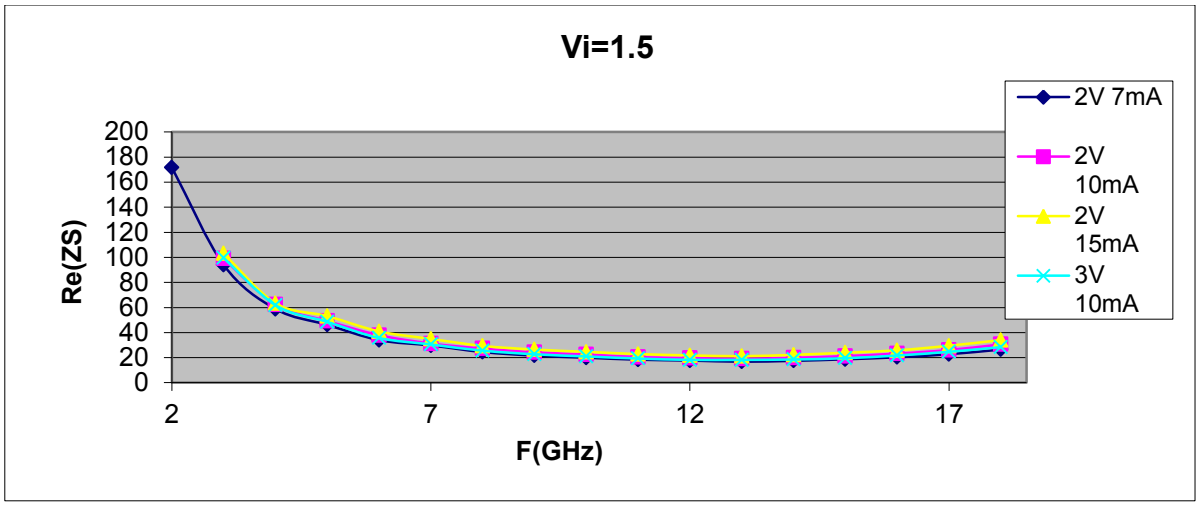


Figure 4. 10 Re{Z_{Sreq}} variation over bandwidth at V_i=1,5 and different quiescent points

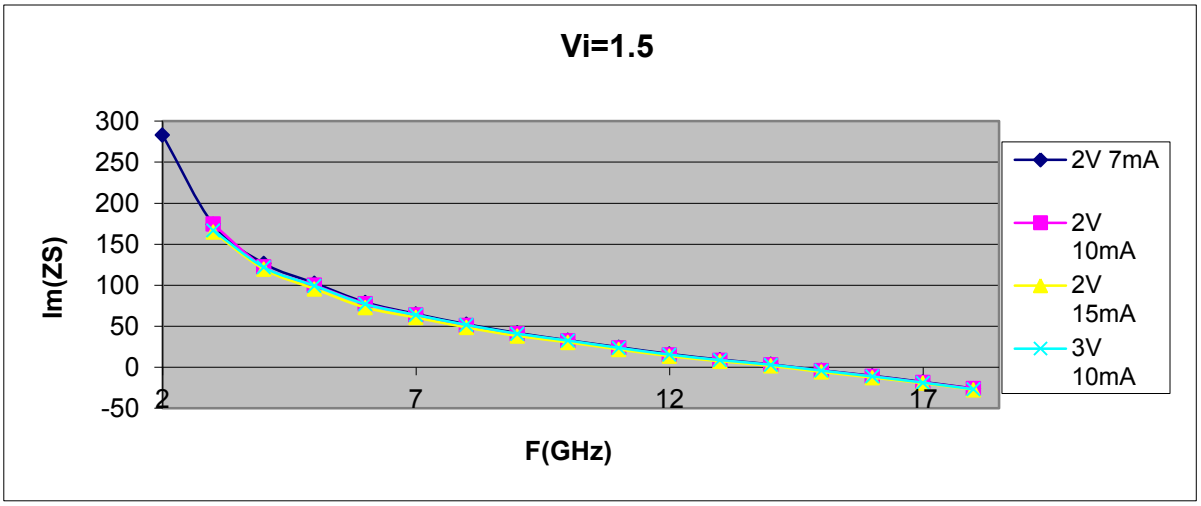


Figure 4. 11 Re{Z_{Sreq}} variation over bandwidth at V_i=1,5 and different quiescent points

Basing on these given figures we had decided to realize an ultra-wideband LNA with NE3503M04 at {V_{DS}=2V|I_{DS}=15mA} quiescent point.

4.2 DC Biasing

Biasing NE3503M04 at {V_{DS}=2V|I_{DS}=15mA} was one of the most important difficulties that had to be overcome.

As a biasing network we had selected double source passive network, applying them on gate and drain ports of the transistor, as show in Figure 3.6 and Table 3.1. By that way we had taken advantage of all positive features of a double source network.

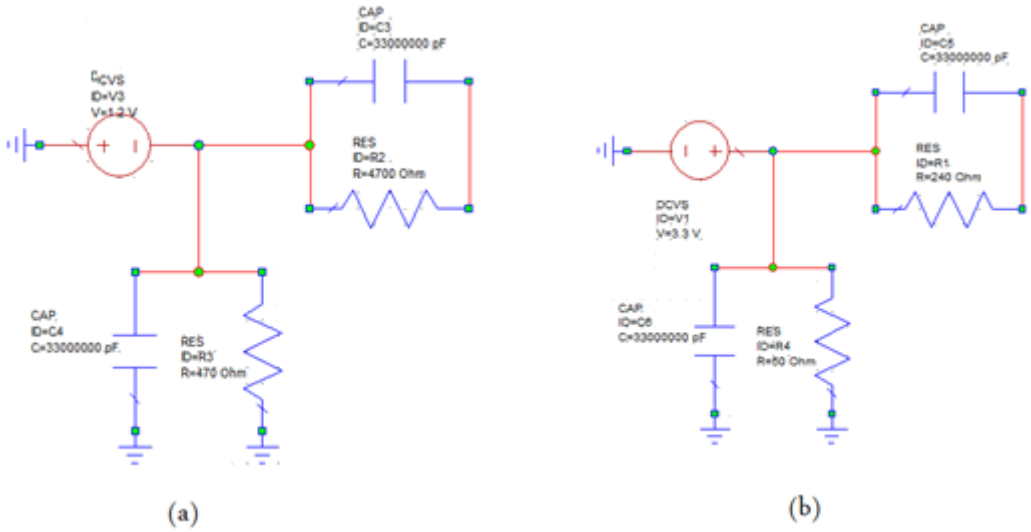


Figure 4. 12 (a) Schematic of a gate biasing network employed during realization. (b) Schematic of a drain biasing network employed during realization.

On an N-channel transistor negative voltage, relative to the ground, must be apply onto gate port of the transistor prior to applying positive voltage to the drain. Else, the overload of drain current may burn out the transistor.

As for RF chocking we have employed chip inductors and microstrip lines. Because an inductor's impedance increases with frequency, we had used Coilcraft 0402HP-2N2XJL_ with 15.1 f_{res} for RF chocking at low frequencies of the bandwidth.

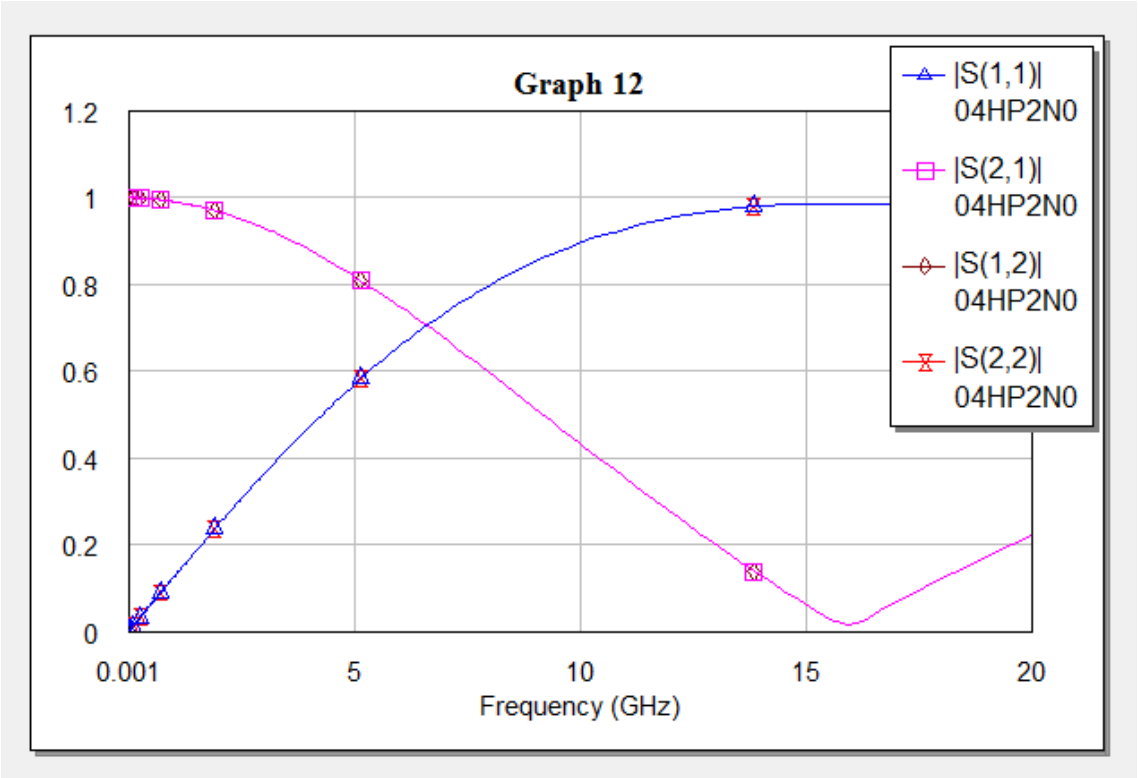


Figure 4. 13 S parameter characterization of the Coilcraft 0402HP-2N2XJL_

4.3 Matching Circuits

During design of the matching circuits several types of matching circuits were researched. Not to add extra noise to the overall noise performance of the circuit, we had refrained from employing multistage matching circuits.

For optimization of the matching circuits I particle swarm optimization developed in [2]. The T type matching circuit had shown best performance and was implemented on both sides the transistor, as shown in Figure 4.14.

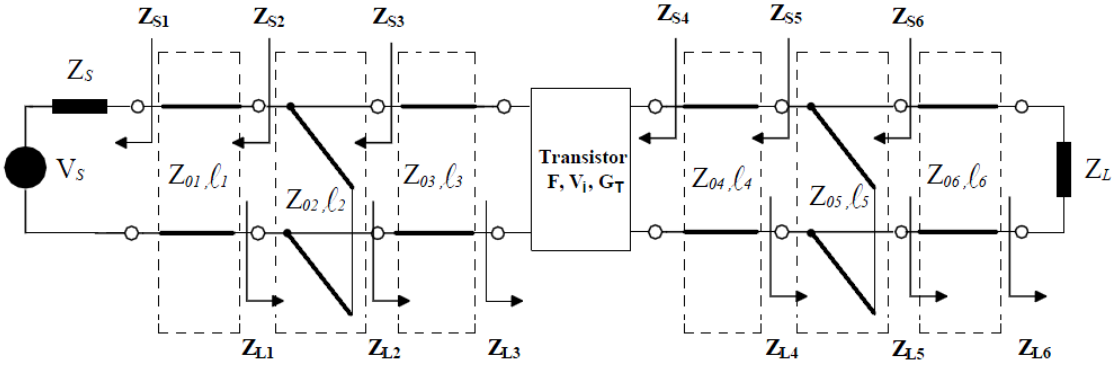


Figure 4. 14 T type matching networks on single-stage amplifier

Following figures were found:

IMC	L_1	W_1	L_2	W_2	L_3	W_3
(mm)	25	0.4321	1.043	0.301	1.362	0.476
OMC	L_4	W_4	L_5	W_5	L_6	W_6
(mm)	3.577	1.125	0.9685	1.446	3.657	0.955

4.4 Realization

During simulation and realization of the circuit following components where used:

Substrate: RO4003C

Transistor: HJ-FET NE3503M04

Inductor: Coilcraft 0402HP-2N2XJL_ (2.2nF)

Capacitor: ATC 500S Series BMC 0402 (33pF)

Connectors: SMA

At the simulations following graphs were generated by AWR Microwave Office program.

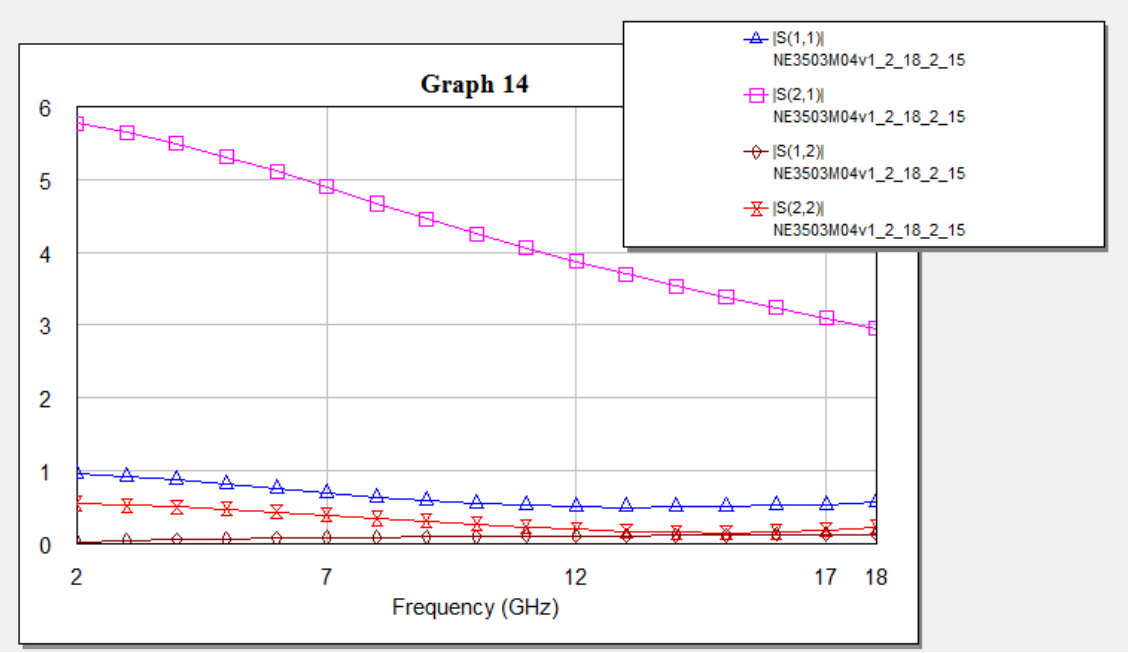


Figure 4. 15 S parameter variation of the NE3503M04

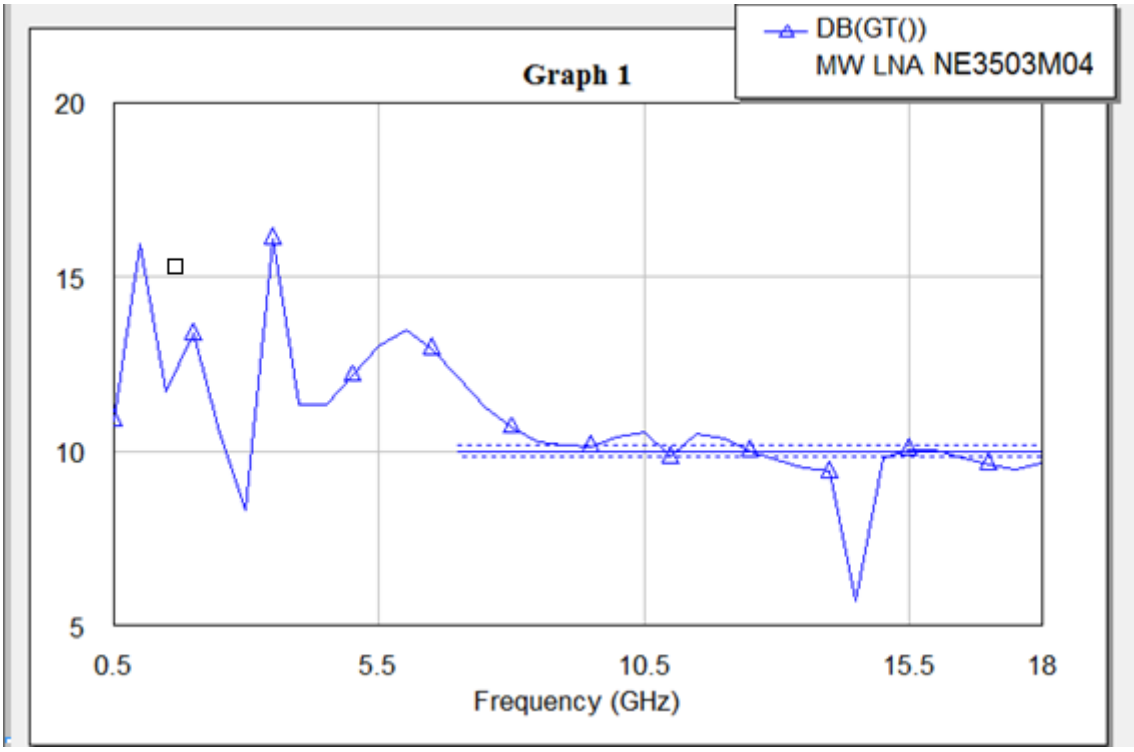


Figure 4. 16 Simulated gain

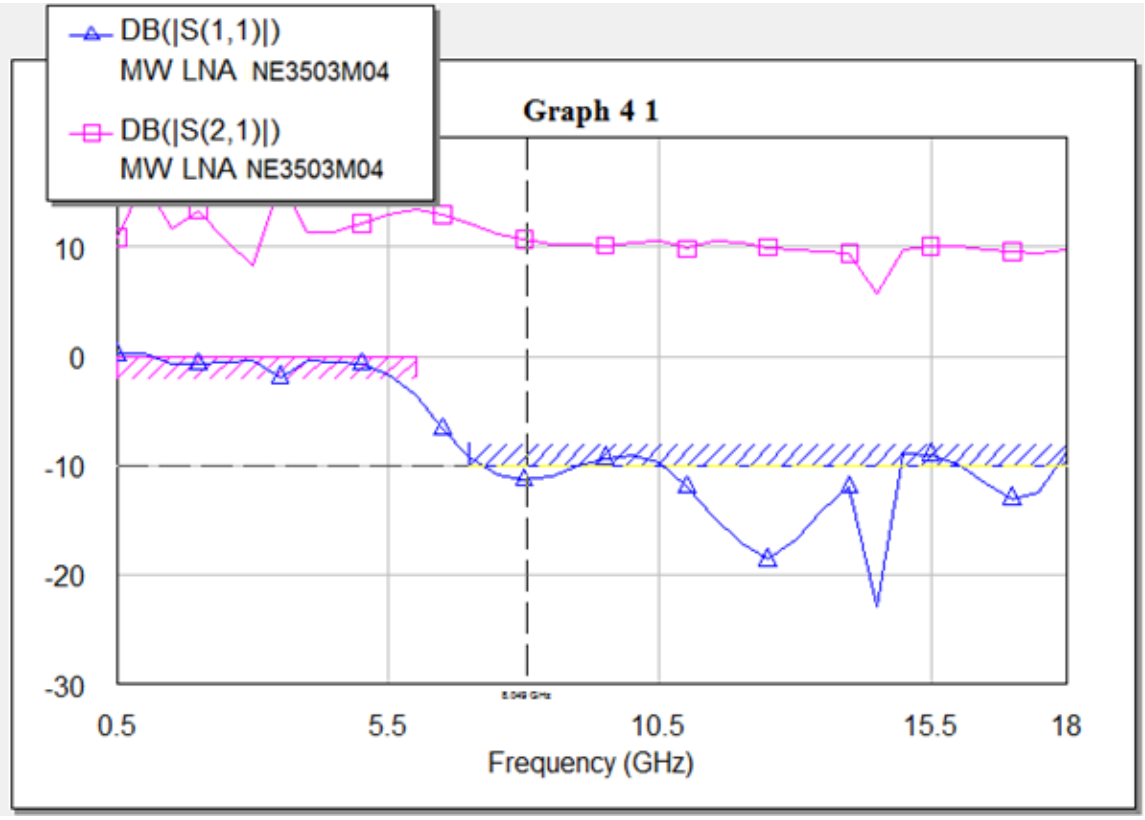


Figure 4. 17 Simulated S (1,1) and S(2,1) variations

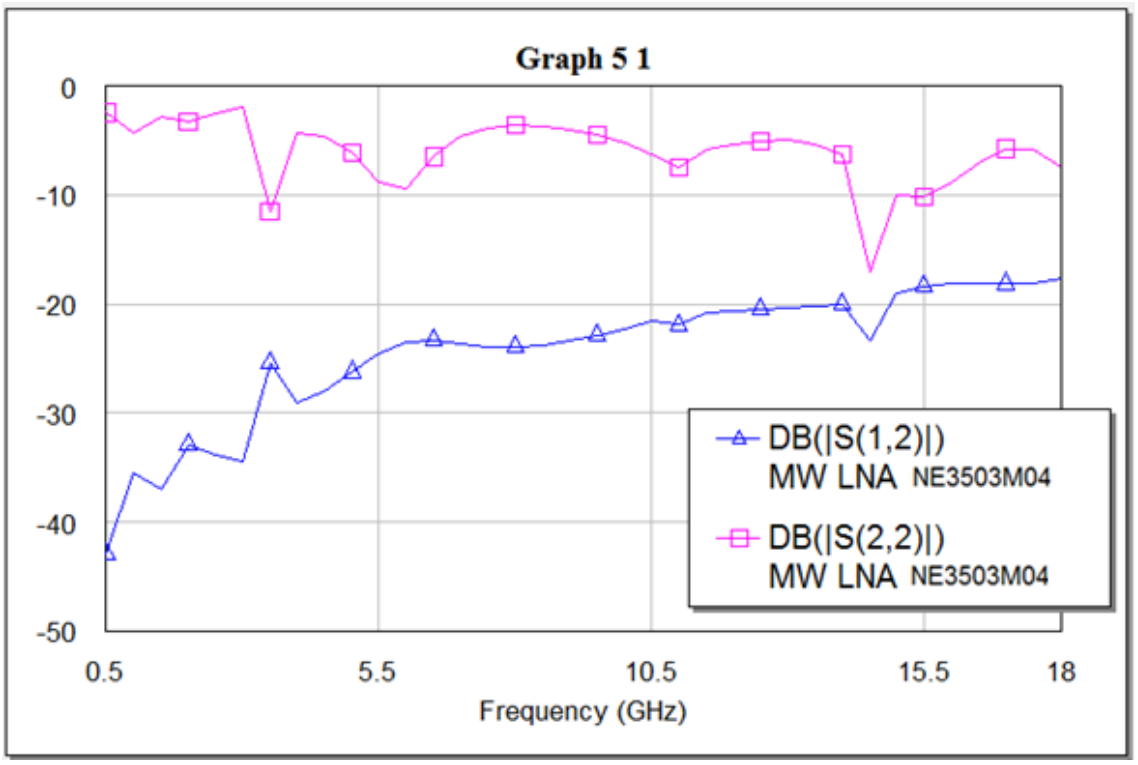


Figure 4. 18 Simulated S (1,2) and S(2,2) variations

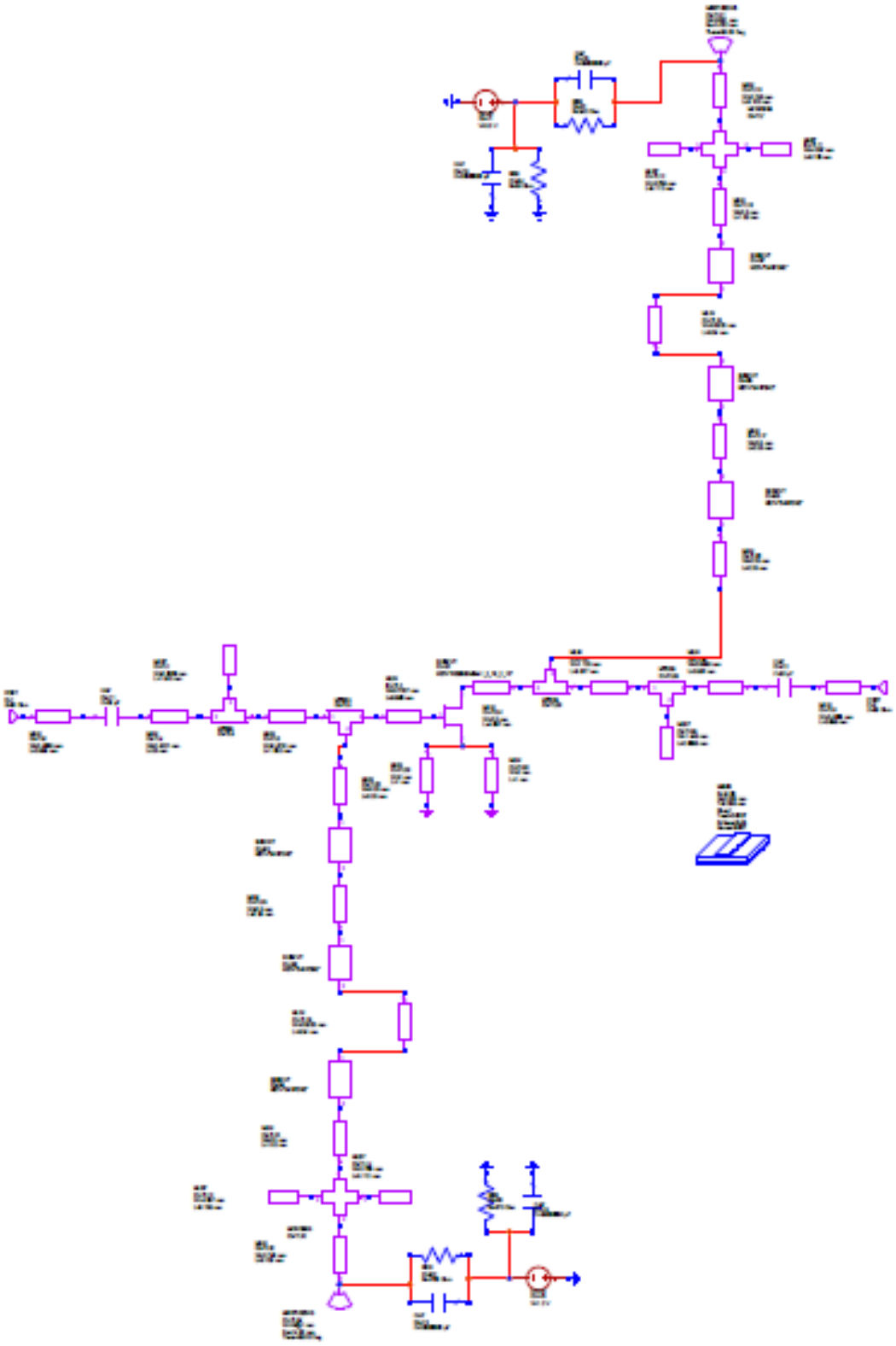


Figure 4. 19 Schematic view of the circuit

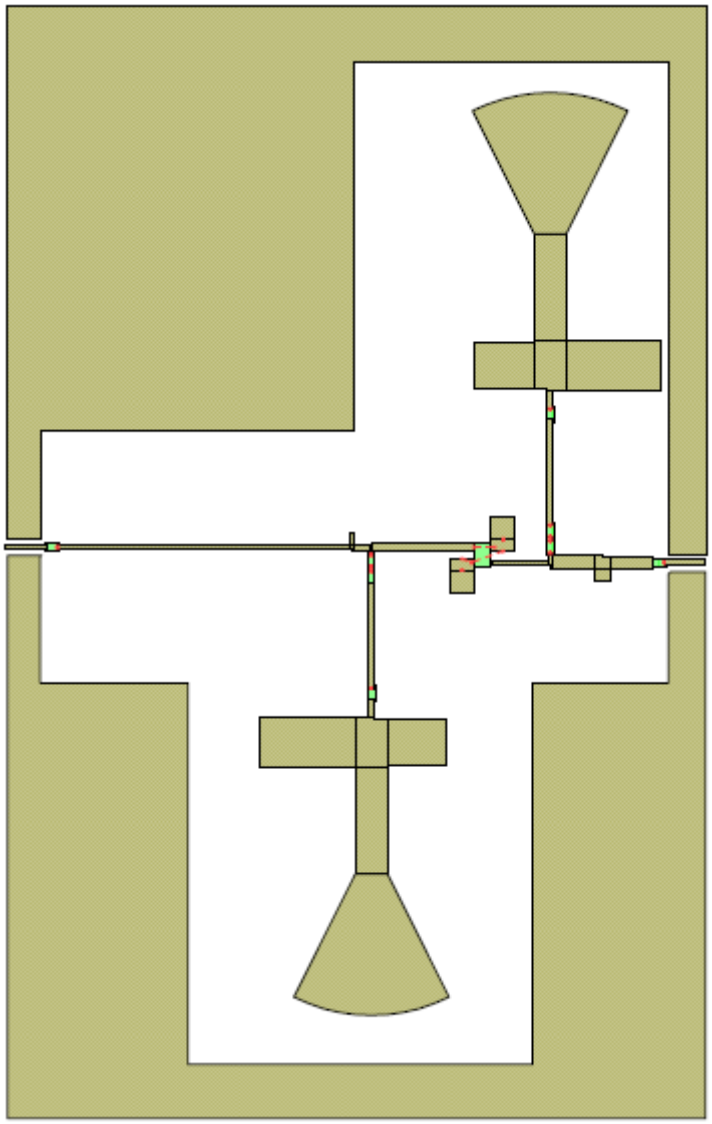


Figure 4. 20 Layout view of the circuit

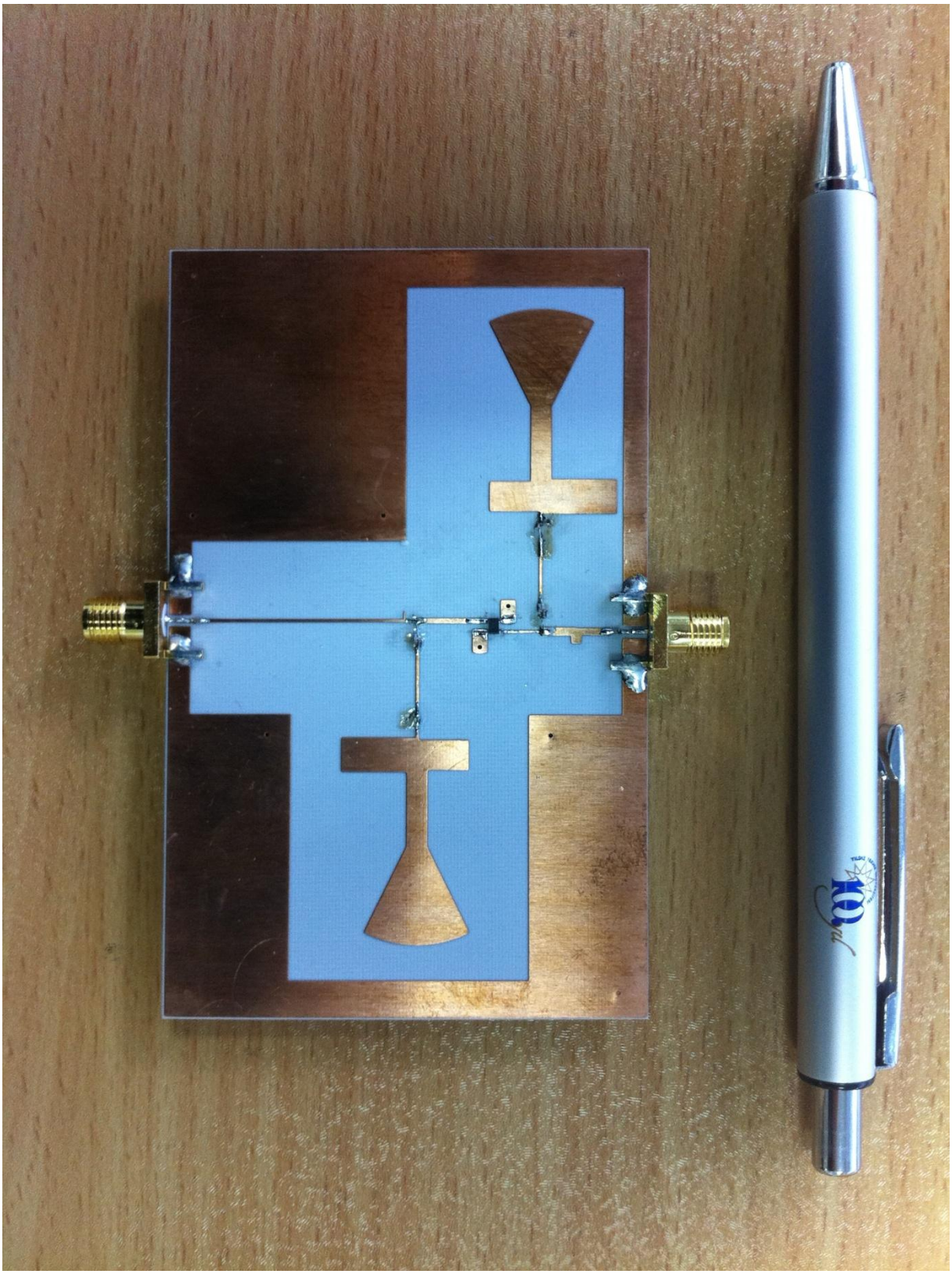


Figure 4. 21 Printed circuit and its relative size to a pen

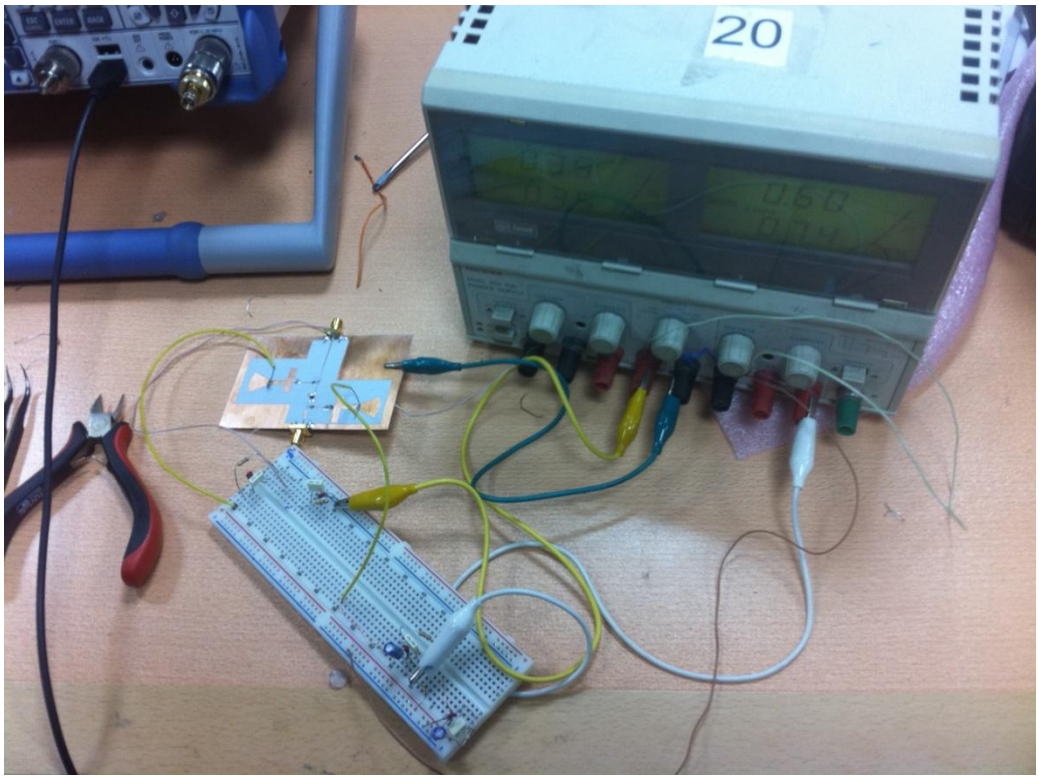


Figure 4. 22 DC biasing circuit with positive and negative bias supply

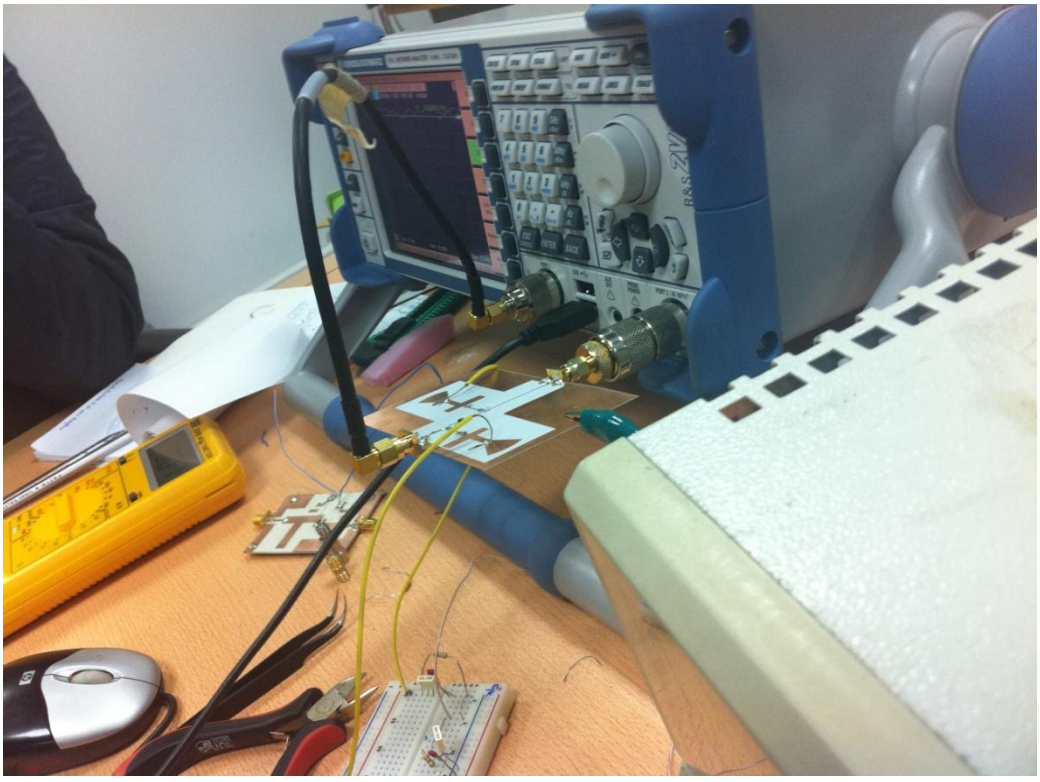


Figure 4. 23 The printed circuit and a network analyzer

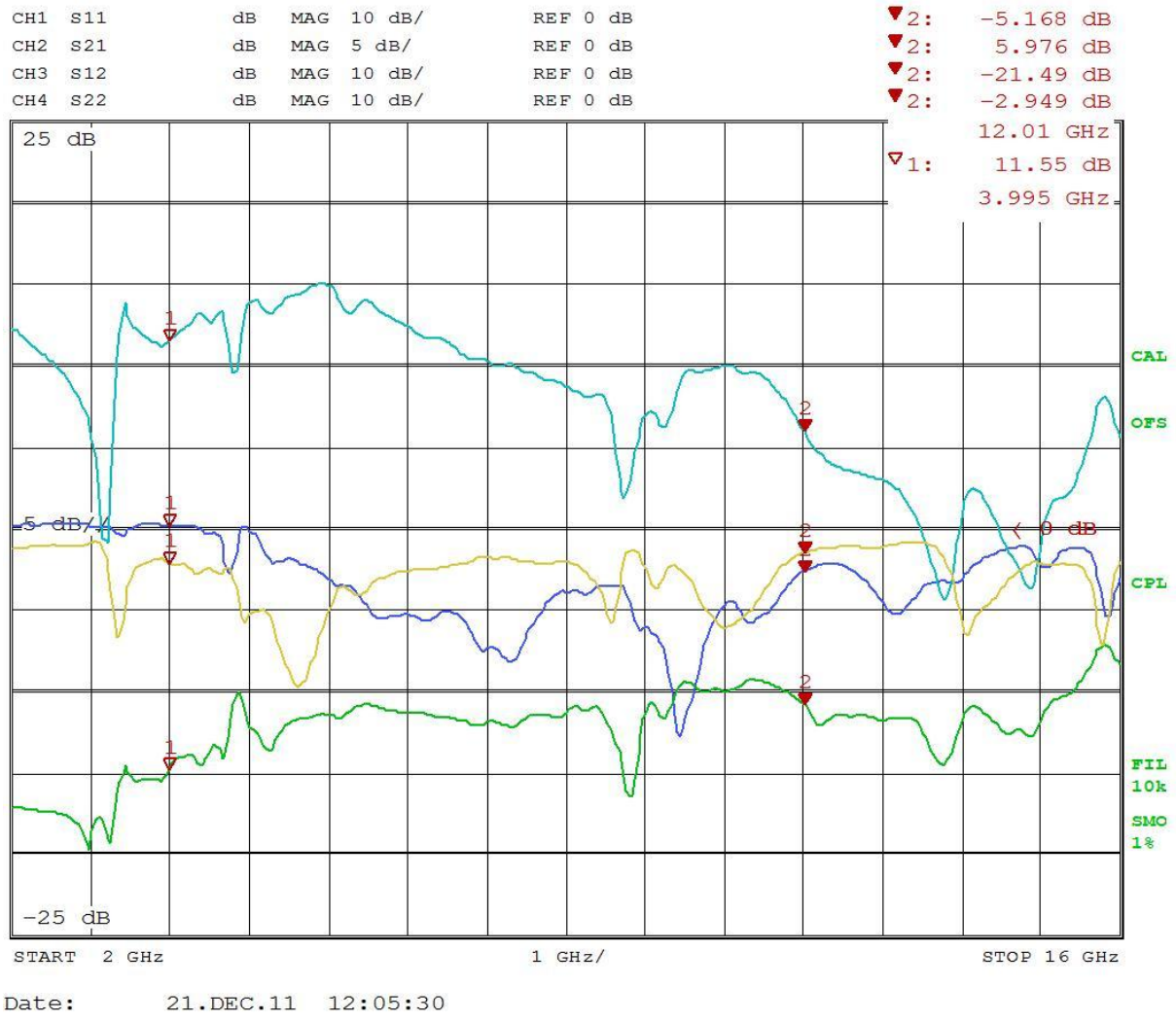


Figure 4.24 Measured S parameters of the circuit with reference plane at input and output ports.

In spite of our desire, the network analyzer could only drive input signal from 1 to 16 GHz. Because of it we were not able to measure higher frequencies. The S_{11} of the circuit, with reference plane at input and output ports, had roughly stayed below -6dB over 8GHz bandwidth. The S_{21}, or gain, had roughly stayed at 10dB ±3dB from 3GHz to 12GHZ, plunging at roughly 9,5GHz with less than 400 MHz bandwidth. This can be explained by fabrication misprint and far improper soldering conditions which were available for us. The S_{12} had stayed below -20dB over whole bandwidth. Thus we can confidently say that the circuit is operational.

CONCLUSION

In this paper I presented and focused on theoretical and practical considerations of an amplifier design. The main aim was to keep theoretical background content as far as possible, get down quickly to the main points of the realization.

In the paper it was shown that the complex requirements of ultra and broadband circuits can be confidently overcome by using geometrical approach and PSO. We had successfully realized unconditionally stable LNA with approximately 10dB transducer gain over 8 GHZ bandwidth and S_{11} well below -6dB over wideband.

BIBLIOGRAPHY

[1] Nguen C., (2001). Analysis Methods for RF, Microwave, and Millimeter-wave Planar Transmission Line Structures, John Willey & Sons, Inc., USA.

[2] Demirel S., (2009). Genelleştirilmiş Mikrodalga Kuvvetlendirici Tasarım Prosedürü ve Uygulamaları (Tek Katlı, Çok Katlı Kuvvetlendiriciler), Istanbul.

[3] Bahl I. and Bhartia P., (2003). Microwave Solid State Circuit Design, Second ed., John Willey & Sons, Inc., USA.

[4] Bahl I., (2003). Lumped Elements for RF and Microwave Circuits, Artech House, Inc., Norwood.

[5] Güneş F., Demirel S., and Özkaya U. (2010), "A Low-Noise Amplifier Design Using the Performance Limitions of a Microwave Transistor for the Ultra-Wideband Applications", Wiley Periodicals Inc., 535-545.

[6] Güneş F., Demirel S., and Özkaya U. (2009), "Design of an Ultra-Wideband, Low-Noise Amplifier Using a Single Transistor: a Typical Application Example", Progress in Electromagnetics Research B, 16:371-387.

[7] Güneş F., and Tepe C., (2002). "Gain-bandwidth limitations of microwave transistor", International Journal of RF and Microwave Computer-Aided Engineering, 12(6):483-495.

[8] Güneş F., Türker N., and Gürgen F., (2007). "Signal-noise support vector model of a microwave transistor", International Journal of RF and Microwave Computer-Aided Engineering, 17(4): 404-415.

[9] Güneş F., Özkaya U., and Demirel S., (2009) "Particle swarm intelligence applied to determination of the feasible design target for a low-noise amplifier", Microwave and Optical Technology Letters, 51(5): 1214-1218.

[10] Ismail A., and Abidi A. A., (2004). "A 3-10-gHz Low-Noise Amplifier With Wideband LC-Ladder Matching Network", IEEE journal of Solid-State Circuits, 39(12): 2296-2277.

[11] Güneş F., and Bilgin C., (2008). "A Generalized design Procedure For a Microwave Amplifier: A Tyipcal Application Example", Progress In Electromagnetics Research B, 10:1-19.

[12] Güneş F., Güneş M., and Fidan M.,(1994). "Performance Characterization of a Microwave Transistor", IEE Proc.-Circuits Devices Syst., 141(5): 337-344

[13] Güneş F., and Çetiner B.A., (1998). "Smith Chart Formulation of Performance Characterization For a Microwave Transistor", IEE Proc.-Circuits Devices Syst., 145(6): 419-428

[14] Virdee B. S., Virdee A. S., and Banyamin B. Y., (2004). Broadband Microwave Amplifiers, Artech House, Inc., Boston&London.

[15] Gonzalez G., (1997). Microwave Transistor Amplifiers: Analysis and Design, Prentice-Hall Inc., USA.

[16] Holzman E., (2006). Essential of RF and Microwave Grounding, Artech House, Inc., Boston&London.

[17] Bowick C., Blyler J., and Ajluni C., (2008). RF Circuit Design, Elsevier Inc., Oxford.

[18] Gupta K.C., Bahl I., Bhartia P., and Garg R., (1996). Microstrip Lines and Slotlines, Second ed., Artech House, Inc., Boston&London.

[19] Vendelin G. D., Pavio A. M., and Rohde U. L., (2005). Microwave Circuit Design Using Linear and Nonlinear Techniques, Second ed., John Willey & Sons, Inc., New Jersey.

[20] Coilcraft, Critical Products and Services http://www.coilcraft.com/ , 06 September 2010

[21] Electronic Component's Date Sheet Search Cite, http://www.alldatasheep.com/, 11 July 2010

CURRICULUM VITAE

Personal Information

Name Surname : Arslan CHARIYEV

Date and Place of Birth : 10.02.1986/Turkmenistan

Foreign Language : Turkish, English, and Russian

E-mail : arslanbtk@hotmail.com

Education

Degree	Field	School/University	Graduated
Bachelors	Electronics and Com.	Yıldız Technical Uni.	2007
Secondary		Turkmen-Turkish High Sch.	2002